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Analog Switches

ON Semiconductor

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For additional information, please contact your local
Sales Representative.

Table of Contents

Analog Switches

Analog switches have been offered by ON Semiconductor (formerly SCG of Motorola) as part of the Logic operations product offering for over 20 years. They continue to be part of the standard logic family portfolios for Metal Gate, High–Speed, Very High–Speed, LVX, and most recently, VHC One–Gate.

These analog switches, come in a variety of functions and have played a very important role in providing system design support in many market segments. Functions ranging from data selectors and SPST switches, to multiple–channel multiplexer/demultiplexers continue to gain popularity. They perform unique and important functions in applications such as audio or video signal switching, A/D converter multiplexing, or RF signal switching. In addition, analog switches are frequently used as relays (minimal signal delays), or simply to provide bilateral isolation between circuits.

System designers also use analog switches to address signal routing issues or to allow for "hot swapping" capability of individual devices and system boards.

New Analog Switch Products

Throughout the industry, popular analog switch functions are offered in practically all of the standard logic families, to take advantage of technology improvements and to facilitate interfacing analog switch functions to changes in system design. ON Semiconductor continues to include them as part of logic family portfolios, and very recently added the first two One–Gate analog switches. Plans are in place to add additional functions to this and the other low–voltage families offered by ON Semiconductor.

Eleven, recently introduced devices–MC74LVX4066, 8051, 8053 and their TTL compatible versions (MC74LVXT4066, 8051, 8053), three new VHC products–MC74VHC4051, 4052, 4053, and two new One–Gate devices–MC74VHC1G66/1GT66, round out the current ON Semiconductor offering. These new devices compliment the standard offering of analog switch multiplexer/de–multiplexers. They are single supply devices from 2.0 to 6.0 volts for the standard CMOS parts and 5.0 volts for the TTL–compatible versions. Typical resistance values are less than 15 Ω for many of the devices when operating at 5.0 volts. The multi–gate, standard family products are available in both SOIC and TSSOP 16–lead packages, while the One–Gate devices are available in the industry standard SC–88A/SC–70 5 lead, SOT–353 packages.

New Analog Switch Data Book

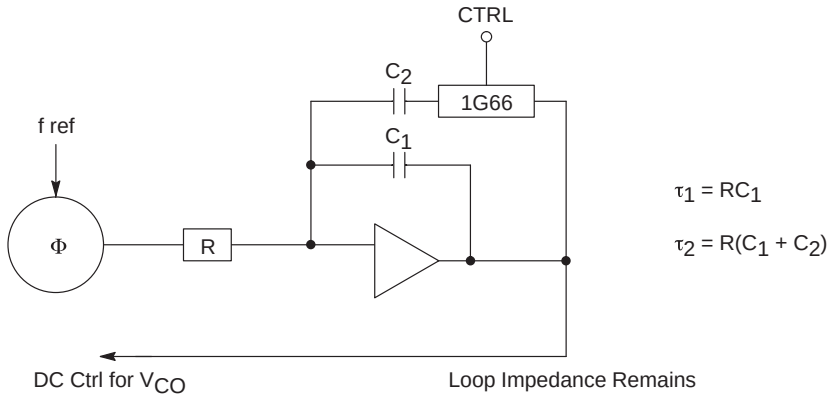
The purpose of providing this new Analog Switch Data Book is to capture the entire portfolio offering of analog switches from the ON Semiconductor Logic Division in a single publication and to provide a vehicle for promoting additional planned introductions. It is our intent to provide easy access to information regarding all of ON Semiconductor's analog switch products.

Many Diverse Applications: Analog switches can be used in many ways to accomplish switching, multiplexing/de–multiplexing of both analog and digital signals. Many so–called digital signals are actually quasi–analog in nature, such as FSK (frequency shift key), PSK (phase–shift key), QAM (Quadrature Amplitude Modulation), CDMA (Code Division Multiplex, and TDMA (Time Division Multiplexing). They need to share the decoding from several different input sources, while inserting minimum signal distortion. When switching signals between 2 or more items in consumer product applications, analog switches play a key role.

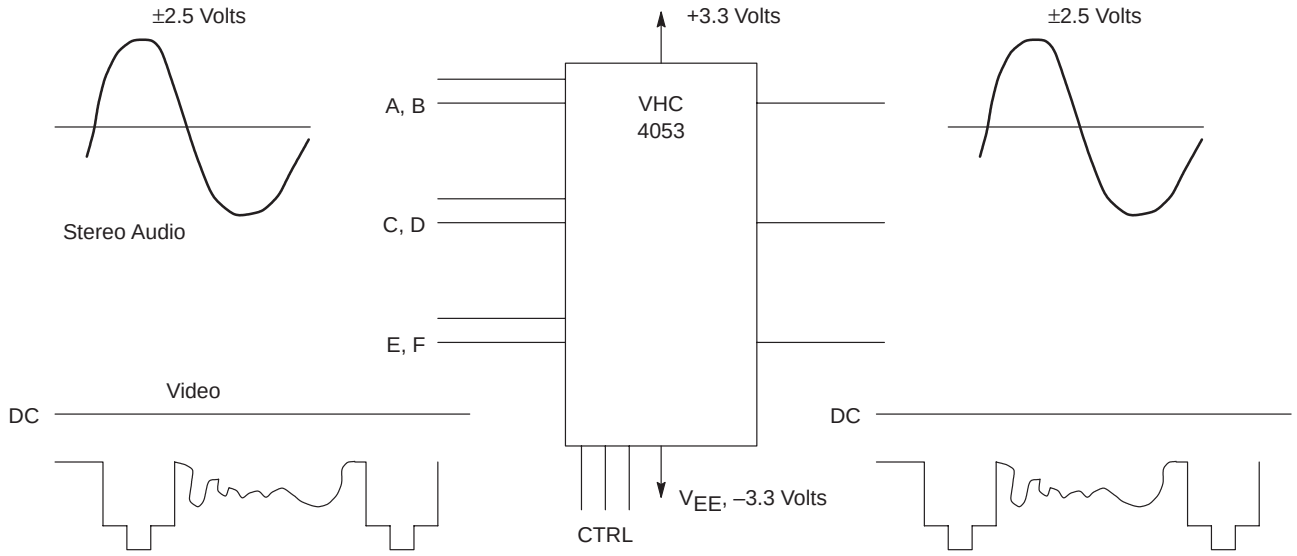
ON Semiconductor recently introduced two additional devices in the advanced high–speed, sub–micron VHC One–Gate, CMOS family. The MC74VHC1G66 and MC74VHC1GT66 devices offer a single analog switch function with impressive AC performance levels.

Analog Switch Applications:

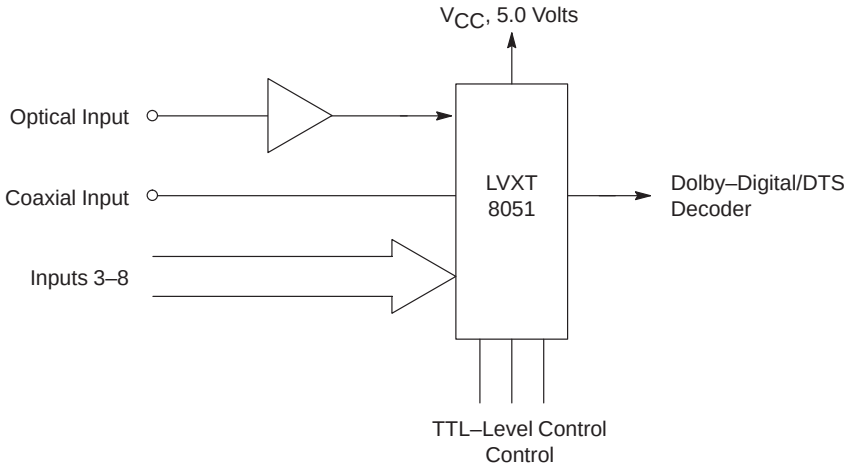
Application 1: Change a time constant in a loop filter application, for fast "attack" stable "hold"



Application 2: The three new VHC devices, MC74VHC4051, MC74VHC4052, MC74VHC4053 provide improved performance and allow operation with both positive and negative supplies. This feature allows for switching an AC waveform that is centered around zero volts with no coupling capacitors. With a +/– 3.3 volt supply, video signals can be switched, while preserving the dc component of its signal. The +/– 3.3 volt supply allows for a 5 volt peak–to–peak waveform, with LVTTL/CMOS compatibility. The d.c. level is preserved, for the case of video switching. The VHC4053 is useful for switching beyond 30 MHz. The following diagram illustrates switching two audio channels from 2 sources and 2 video channels simultaneously. The signal levels may be +/– 2.5 volts.



Application 3: Select between one of eight sources to decode for a Dolby Digital or DTS Decoder. A stereo receiver will likely have a single audio decoder, but will need to switch between several possible inputs– optical and coaxial. The MC74LVX8051 will allow the designer to switch between up to 8 inputs to be connected to a single (expensive) decoder. The de–multiplexer is low cost, and adds minimum loss and distortion to the circuit. The frequency that it needs to handle is in the 10 MHz range.



Note: DTS and Dolby Digital are trademarks of their respective companies

Data Sheets

MC14016B

Quad Analog Switch/ Quad Multiplexer

The MC14016B quad bilateral switch is constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. Each MC14016B consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise — 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1.0 kHz typical
- Pin–for–Pin Replacements for CD4016B, CD4066B (Note improved transfer characteristic design causes more parasitic coupling capacitance than CD4016)
- For Lower R_{ON}, Use The HC4016 High–Speed CMOS Device or The MC14066B
- This Device Has Inputs and Outputs Which Do Not Have ESD Protection. Antistatic Precautions Must Be Taken.

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	–0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	–0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient) per Control Pin	±10	mA
I_{SW}	Switch Through Current	±25	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	–55 to +125	°C
T_{stg}	Storage Temperature Range	–65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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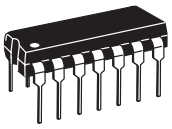
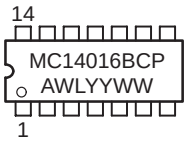
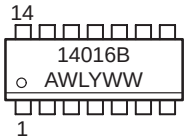
MARKING DIAGRAMS

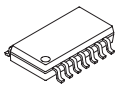


PDIP–14
P SUFFIX
CASE 646

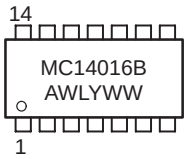


SOIC–14
D SUFFIX
CASE 751A





SOEIAJ–14
F SUFFIX
CASE 965



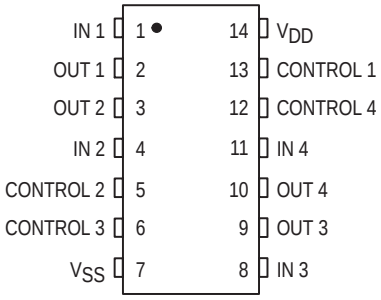
A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

ORDERING INFORMATION

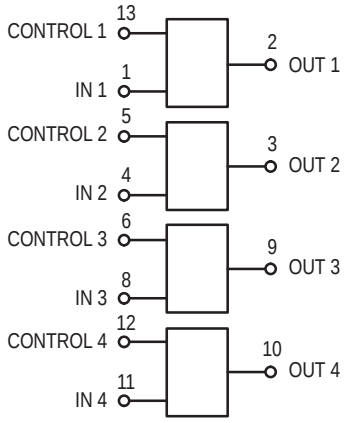
Device	Package	Shipping
MC14016BCP	PDIP–14	2000/Box
MC14016BD	SOIC–14	55/Rail
MC14016BDR2	SOIC–14	2500/Tape & Reel
MC14016BF	SOEIAJ–14	See Note 1.
MC14016BFEL	SOEIAJ–14	See Note 1.
MC14016BFR1	SOEIAJ–14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT



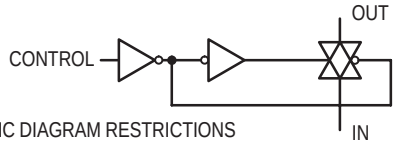
BLOCK DIAGRAM



V_{DD} = PIN 14
V_{SS} = PIN 7

Control	Switch
0 = V_{SS}	Off
1 = V_{DD}	On

LOGIC DIAGRAM
(1/4 OF DEVICE SHOWN)



LOGIC DIAGRAM RESTRICTIONS
$V_{SS} \le V_{in} \le V_{DD}$
$V_{SS} \le V_{out} \le V_{DD}$

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Figure	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Input Voltage Control Input	1	V_{IL}	5.0 10 15	— — —	— — —	— — —	1.5 1.5 1.5	0.9 0.9 0.9	— — —	— — —	Vdc
		V_{IH}	5.0 10 15	— — —	— — —	3.0 8.0 13	2.0 6.0 11	— — —	— — —	— — —	Vdc
Input Current Control	—	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	± 1.0	µAdc
Input Capacitance Control Switch Input Switch Output Feed Through	—	C_{in}	 — — — —	 — — — —	 — — — —	 — — — —	 5.0 5.0 5.0 0.2	 — — — —	 — — — —	 — — — —	pF
Quiescent Current (Per Package) (5.)	2,3	I_{DD}	5.0 10 15	— — —	0.25 0.5 1.0	— — —	0.0005 0.0010 0.0015	0.25 0.5 1.0	— — —	7.5 15 30	µAdc
"ON" Resistance ($V_C = V_{DD}$, R_L = 10 kΩ) (V_{in} = + 5.0 Vdc) (V_{in} = – 5.0 Vdc) V_{SS} = – 5.0 Vdc (V_{in} = ± 0.25 Vdc) (V_{in} = + 7.5 Vdc) (V_{in} = – 7.5 Vdc) V_{SS} = – 7.5 Vdc (V_{in} = ± 0.25 Vdc) (V_{in} = + 10 Vdc) (V_{in} = + 0.25 Vdc) V_{SS} = 0 Vdc (V_{in} = + 5.6 Vdc) (V_{in} = + 15 Vdc) (V_{in} = + 0.25 Vdc) V_{SS} = 0 Vdc (V_{in} = + 9.3 Vdc)	4,5,6	R_{ON}	 5.0 7.5 10 15	 — — — — — — — — — — — — —	 600 600 600 360 360 360 600 600 600 360 360 360	— — — — — — — — — — — — — —	 300 300 280 240 240 180 260 310 310 260 260 300	 660 660 660 400 400 400 660 660 660 400 400 400	— — — — — — — — — — — — — —	 840 840 840 520 520 520 840 840 840 520 520 520	Ohms
Δ "ON" Resistance Between any 2 circuits in a common package ($V_C = V_{DD}$) (V_{in} = ± 5.0 Vdc, V_{SS} = – 5.0 Vdc) (V_{in} = ± 7.5 Vdc, V_{SS} = – 7.5 Vdc)	—	ΔR_{ON}	 5.0 7.5	 — —	 — —	 — —	 15 10	 — —	 — —	 — —	Ohms
Input/Output Leakage Current ($V_C = V_{SS}$) (V_{in} = + 7.5, V_{out} = – 7.5 Vdc) (V_{in} = – 7.5, V_{out} = + 7.5 Vdc)	—	—	 7.5 7.5	 — —	 ±0.1 ±0.1	 — —	 ±0.0015 ±0.0015	 ±0.1 ± 0.1	 — —	 ± 1.0 ± 1.0	µAdc

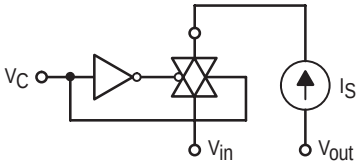
NOTE: All unused inputs must be returned to V_{DD} or V_{SS} as appropriate for the circuit application.

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e., the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.) Reference Figure 14.

ELECTRICAL CHARACTERISTICS (6.) (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD} Vdc	Min	Typ (7.)	Max	Unit
Propagation Delay Time (V_{SS} = 0 Vdc) V_{in} to V_{out} (V_C = V_{DD}, R_L = 10 kΩ)	7	t_{PLH}, t_{PHL}	5.0 10 15	— — —	15 7.0 6.0	45 15 12	ns
Control to Output (V_{in} ≤ 10 Vdc, R_L = 10 kΩ)	8	t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}	 5.0 10 15	 — — —	 34 20 15	 90 45 35	ns
Crosstalk, Control to Output (V_{SS} = 0 Vdc) (V_C = V_{DD}, R_{in} = 10 kΩ, R_{out} = 10 kΩ, f = 1.0 kHz)	9	—	5.0 10 15	— — —	30 50 100	— — —	mV
Crosstalk between any two switches (V_{SS} = 0 Vdc) (R_L = 1.0 kΩ, f = 1.0 MHz, crosstalk = $20\log_{10}\frac{V_{out1}}{V_{out2}}$)	—	—	5.0	—	– 80	—	dB
Noise Voltage (V_{SS} = 0 Vdc) (V_C = V_{DD}, f = 100 Hz) (V_C = V_{DD}, f = 100 kHz)	10,11	—	5.0 10 15 5.0 10 15	— — — — — —	24 25 30 12 12 15	— — — — — —	nV/$\sqrt{\text{Cycle}}$
Second Harmonic Distortion (V_{SS} = – 5.0 Vdc) (V_{in} = 1.77 Vdc, RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	—	—	5.0	—	0.16	—	%
Insertion Loss (V_C = V_{DD}, V_{in} = 1.77 Vdc, V_{SS} = – 5.0 Vdc, RMS centered = 0.0 Vdc, f = 1.0 MHz) I_{loss} = $20\log_{10}\frac{V_{out}}{V_{in}}$) ($R_L$ = 1.0 kΩ) (R_L = 10 kΩ) (R_L = 100 kΩ) (R_L = 1.0 MΩ)	12	—	5.0	 — — —	 2.3 0.2 0.1 0.05	 — — —	dB
Bandwidth (– 3.0 dB) (V_C = V_{DD}, V_{in} = 1.77 Vdc, V_{SS} = – 5.0 Vdc, RMS centered @ 0.0 Vdc) (R_L = 1.0 kΩ) (R_L = 10 kΩ) (R_L = 100 kΩ) (R_L = 1.0 MΩ)	12,13	BW	5.0	 — — —	 54 40 38	 — — —	MHz
OFF Channel Feedthrough Attenuation (V_{SS} = – 5.0 Vdc) (V_C = V_{SS}, $20\log_{10}\frac{V_{out}}{V_{in}}$ = –50 dB) (R_L = 1.0 kΩ) (R_L = 10 kΩ) (R_L = 100 kΩ) (R_L = 1.0 MΩ)	—	—	5.0	 — — —	 1250 140 18	 — — —	kHz

6. The formulas given are for typical characteristics only at 25°C.
7. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.



V_{IL}: V_C is raised from V_{SS} until $V_C = V_{IL}$.
at $V_C = V_{IL}$: $I_S = \pm 10\ \mu A$ with $V_{in} = V_{SS}$, $V_{out} = V_{DD}$ or $V_{in} = V_{DD}$, $V_{out} = V_{SS}$.

V_{IH}: When $V_C = V_{IH}$ to V_{DD}, the switch is ON and the R_{ON} specifications are met.

Figure 1. Input Voltage Test Circuit

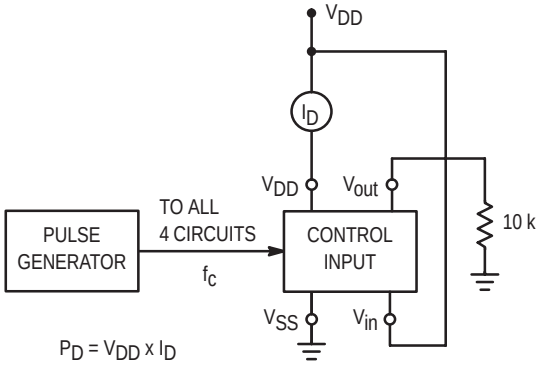


Figure 2. Quiescent Power Dissipation Test Circuit

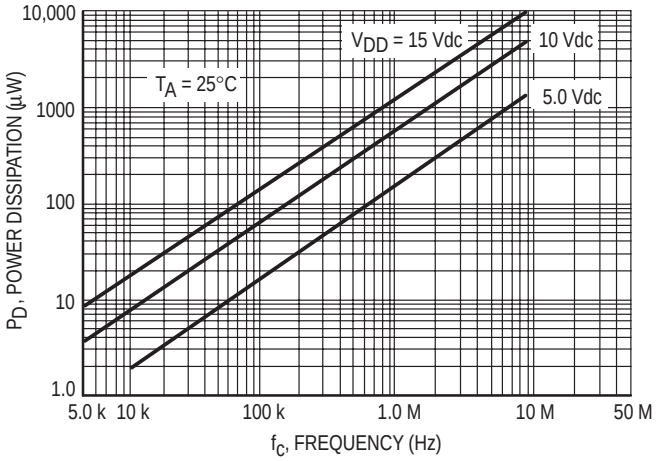


Figure 3. Typical Power Dissipation per Circuit (1/4 of device shown)

TYPICAL R_{ON} versus INPUT VOLTAGE

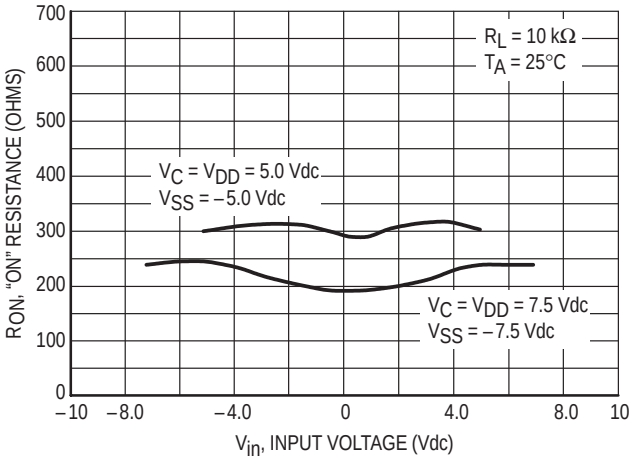


Figure 4. V_{SS} = – 5.0 V and – 7.5 V

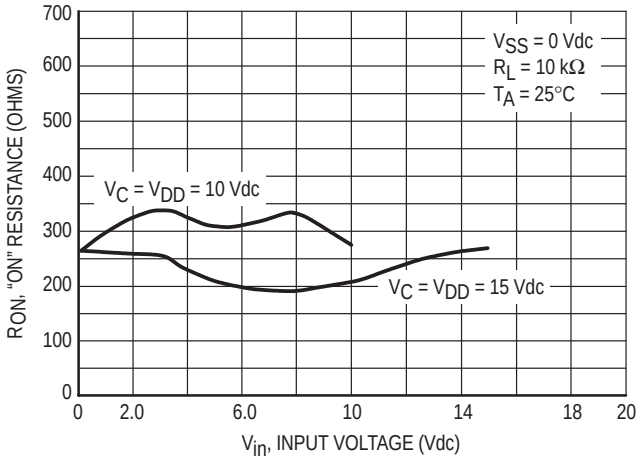


Figure 5. V_{SS} = 0 V

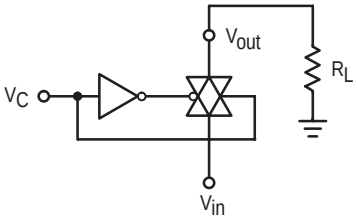


Figure 6. R_{ON} Characteristics Test Circuit

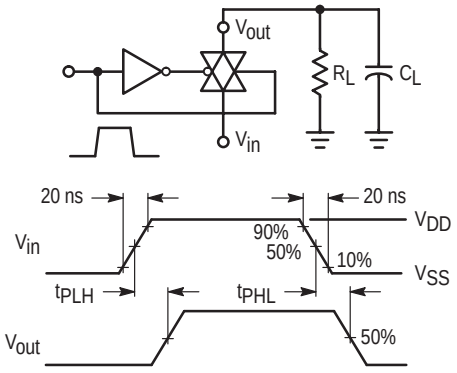


Figure 7. Propagation Delay Test Circuit and Waveforms

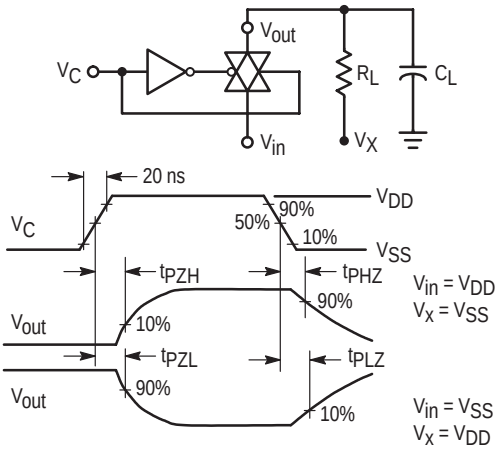


Figure 8. Turn–On Delay Time Test Circuit and Waveforms

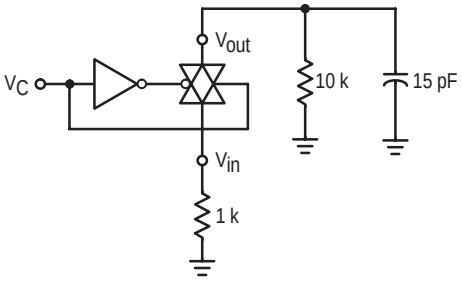


Figure 9. Crosstalk Test Circuit

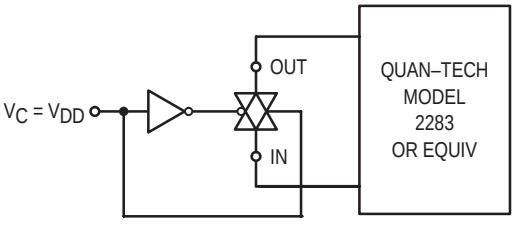


Figure 10. Noise Voltage Test Circuit

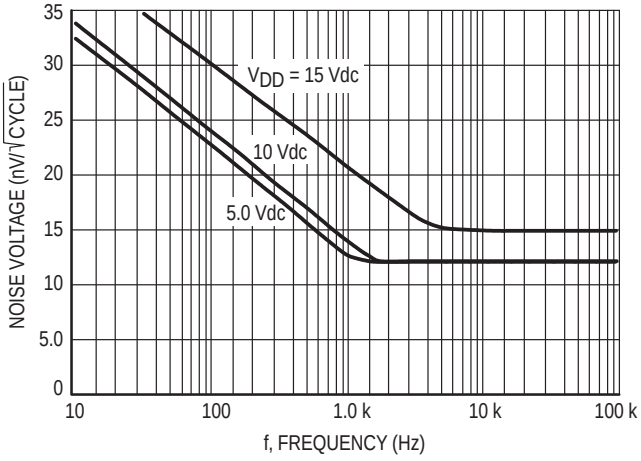


Figure 11. Typical Noise Characteristics

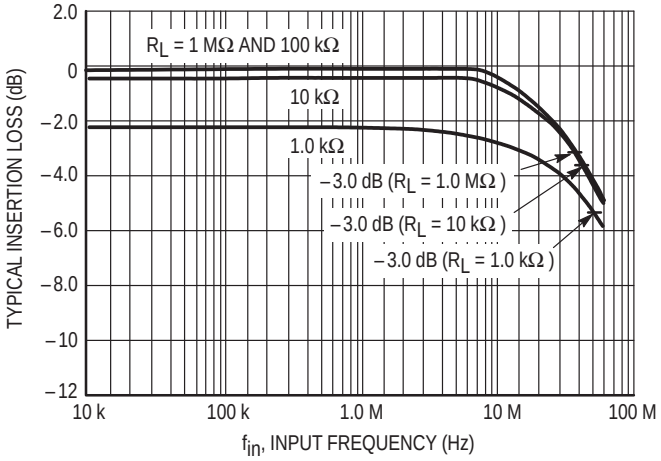


Figure 12. Typical Insertion Loss/Bandwidth Characteristics

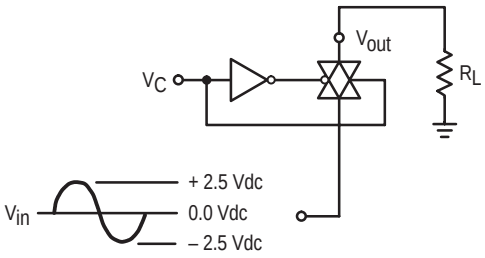


Figure 13. Frequency Response Test Circuit

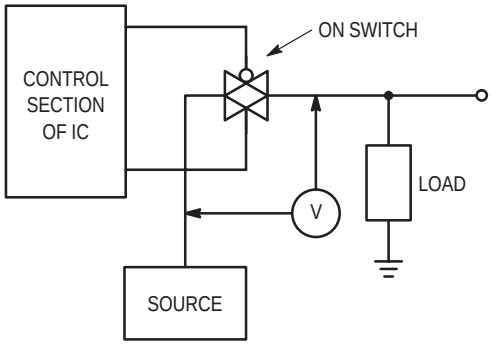


Figure 14. ΔV Across Switch

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0–to–5 V Digital Control signal is used to directly control a 5 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = +5 V logic high at the control inputs; V_{SS} = GND = 0 V logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS}. The analog voltage must not swing higher than V_{DD} or lower than V_{SS}.

The example shows a 5 V_{p-p} signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_X) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{SS} is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{SS}.

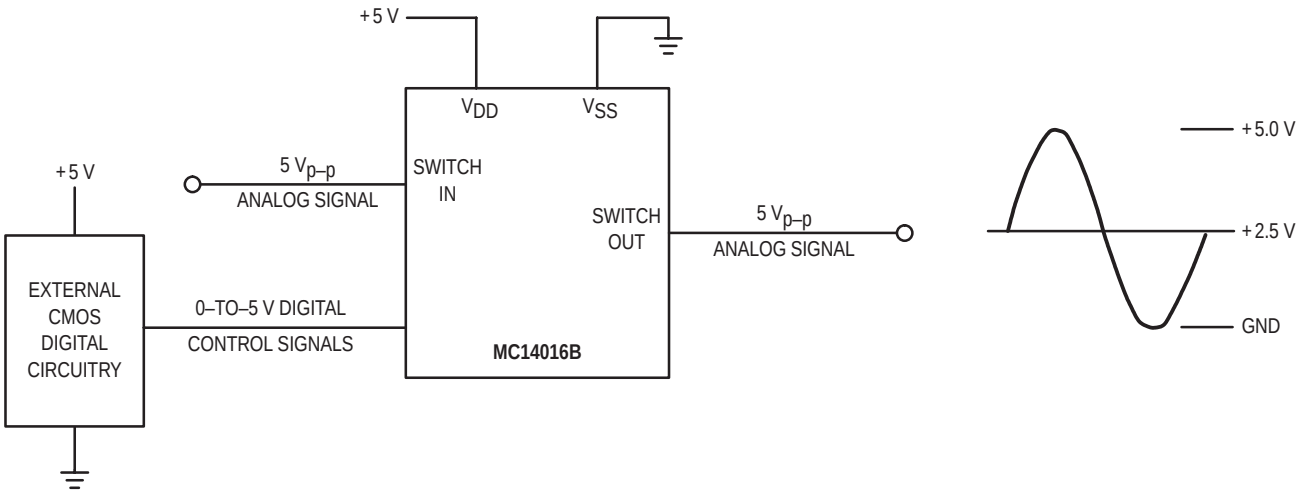


Figure A. Application Example

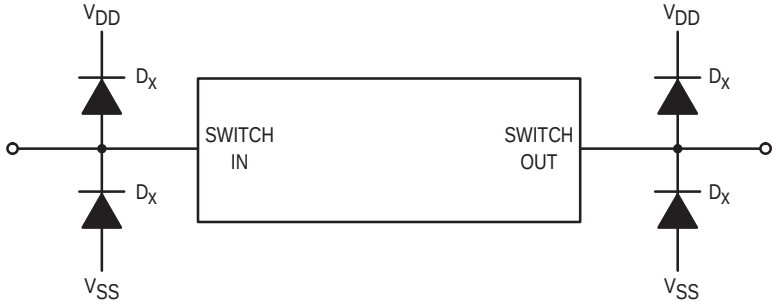


Figure B. External Germanium or Schottky Clipping Diodes

MC14051B, MC14052B, MC14053B

Analog Multiplexers/Demultiplexers

The MC14051B, MC14052B, and MC14053B analog multiplexers are digitally–controlled analog switches. The MC14051B effectively implements an SP8T solid state switch, the MC14052B a DP4T, and the MC14053B a Triple SPDT. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- Triple Diode Protection on Control Inputs
- Switch Function is Break Before Make
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range ($V_{DD} – V_{EE}$) = 3.0 to 18 V
  Note: V_{EE} must be $\leq V_{SS}$
- Linearized Transfer Characteristics
- Low–noise – 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1.0 kHz Typical
- Pin–for–Pin Replacement for CD4051, CD4052, and CD4053
- For 4PDT Switch, See MC14551B
- For Lower R_{ON}, Use the HC4051, HC4052, or HC4053 High–Speed CMOS Devices

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{EE}, $V_{SS} \geq V_{EE}$)	–0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient) (Referenced to V_{SS} for Control Inputs and V_{EE} for Switch I/O)	–0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient) per Control Pin	±10	mA
I_{SW}	Switch Through Current	±25	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Ambient Temperature Range	–55 to +125	°C
T_{stg}	Storage Temperature Range	–65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS}, V_{EE} or V_{DD}). Unused outputs must be left open.

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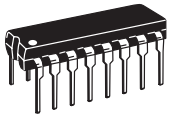
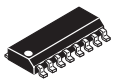
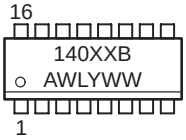
MARKING DIAGRAMS



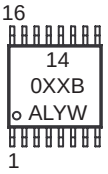
PDIP–16
P SUFFIX
CASE 648

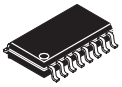


SOIC–16
D SUFFIX
CASE 751B

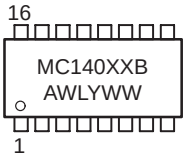


TSSOP–16
DT SUFFIX
CASE 948F





SOEIAJ–16
F SUFFIX
CASE 966

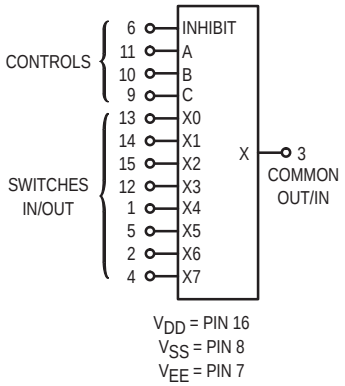


XX = Specific Device Code
A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

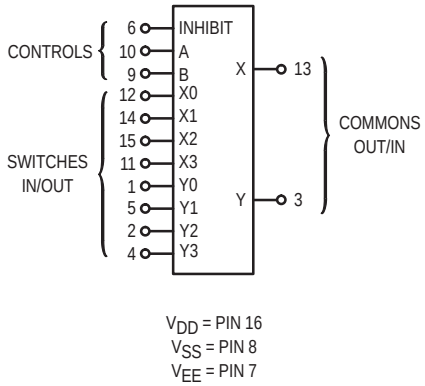
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 24 of this data sheet.

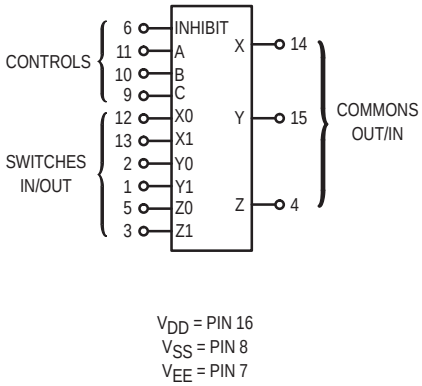
MC14051B
8–Channel Analog Multiplexer/Demultiplexer



MC14052B
Dual 4–Channel Analog Multiplexer/Demultiplexer



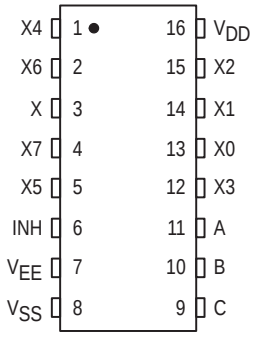
MC14053B
Triple 2–Channel Analog Multiplexer/Demultiplexer



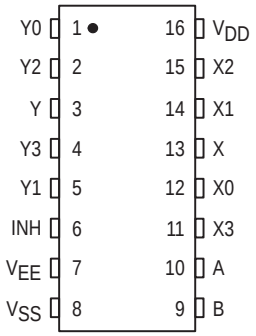
Note: Control Inputs referenced to V_{SS}, Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be ≤ V_{SS}.

PIN ASSIGMENT

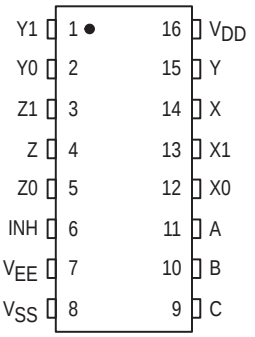
MC14051B



MC14052B



MC14053B



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (3.)	25°C Max	125°C Min	125°C Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	V_{DD}	—	$V_{DD} - 3.0 \geq V_{SS} \geq V_{EE}$	3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I_{DD}	5.0 10 15	Control Inputs: $V_{in} = V_{SS}$ or V_{DD}, Switch I/O: $V_{EE} \leq V_{I/O} \leq V_{DD}$, and $\Delta V_{switch} \leq 500$ mV (4.)	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package	$I_{D(AV)}$	5.0 10 15	$T_A = 25°C$ only (The channel component, $(V_{in} - V_{out})/R_{on}$, is not included.)	Typical			(0.07 μA/kHz) f + I_{DD} (0.20 μA/kHz) f + I_{DD} (0.36 μA/kHz) f + I_{DD}				μA
CONTROL INPUTS — INHIBIT, A, B, C (Voltages Referenced to V_{SS})											
Low–Level Input Voltage	V_{IL}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High–Level Input Voltage	V_{IH}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I_{in}	15	V_{in} = 0 or V_{DD}	—	± 0.1	—	±0.00001	± 0.1	—	1.0	μA
Input Capacitance	C_{in}	—		—	—	—	5.0	7.5	—	—	pF
SWITCHES IN/OUT AND COMMONS OUT/IN — X, Y, Z (Voltages Referenced to V_{EE})											
Recommended Peak–to–Peak Voltage Into or Out of the Switch	$V_{I/O}$	—	Channel On or Off	0	V_{DD}	0	—	V_{DD}	0	V_{DD}	V_{PP}
Recommended Static or Dynamic Voltage Across the Switch (4.) (Figure 5)	ΔV_{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V_{OO}	—	V_{in} = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R_{on}	5.0 10 15	$\Delta V_{switch} \leq 500$ mV (4.) $V_{in} = V_{IL}$ or V_{IH} (Control), and V_{in} = 0 to V_{DD} (Switch)	— — —	800 400 220	— — —	250 120 80	1050 500 280	— — —	1200 520 300	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5.0 10 15		— — —	70 50 45	— — —	25 10 10	70 50 45	— — —	135 95 65	Ω
Off–Channel Leakage Current (Figure 10)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	± 100	—	± 0.05	± 100	—	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	—	Inhibit = V_{DD}	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	$C_{O/I}$	—	Inhibit = V_{DD} (MC14051B) (MC14052B) (MC14053B)	 — — —	 — — —	 — — —	 60 32 17	 — — —	 — — —	 — — —	pF
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	— —	Pins Not Adjacent Pins Adjacent	— —	— —	— —	0.15 0.47	— —	— —	— —	pF

3. Data labeled “Typ” is not to be used for design purposes, but is intended as an indication of the IC’s potential performance.
4. For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn, i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS (5.) (C_L = 50 pF, T_A = 25°C) ($V_{EE} \le V_{SS}$ unless otherwise indicated)

Characteristic	Symbol	$V_{DD} - V_{EE}$ Vdc	Typ (6.) All Types	Max	Unit
Propagation Delay Times (Figure 6)	t_{PLH}, t_{PHL}				ns
Switch Input to Switch Output (R_L = 10 kΩ)					
MC14051					
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 26.5 ns		5.0	35	90	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 11 ns		10	15	40	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 9.0 ns		15	12	30	
MC14052					ns
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 21.5 ns		5.0	30	75	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 8.0 ns		10	12	30	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 7.0 ns		15	10	25	
MC14053					ns
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 16.5 ns		5.0	25	65	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 4.0 ns		10	8.0	20	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 3.0 ns		15	6.0	15	
Inhibit to Output (R_L = 10 kΩ, $V_{EE} = V_{SS}$) Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level	t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}				ns
MC14051B		5.0	350	700	
		10	170	340	
		15	140	280	
MC14052B		5.0	300	600	ns
		10	155	310	
		15	125	250	
MC14053B		5.0	275	550	ns
		10	140	280	
		15	110	220	
Control Input to Output (R_L = 10 kΩ, $V_{EE} = V_{SS}$)	t_{PLH}, t_{PHL}				ns
MC14051B		5.0	360	720	
		10	160	320	
		15	120	240	
MC14052B		5.0	325	650	ns
		10	130	260	
		15	90	180	
MC14053B		5.0	300	600	ns
		10	120	240	
		15	80	160	
Second Harmonic Distortion (R_L = 10KΩ, f = 1 kHz) V_{in} = 5 V_{PP}	—	10	0.07	—	%
Bandwidth (Figure 7) (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD}–V_{EE}) p–p, C_L = 50pF 20 Log (V_{out}/V_{in}) = – 3 dB)	BW	10	17	—	MHz
Off Channel Feedthrough Attenuation (Figure 7) R_L = 1KΩ, V_{in} = 1/2 (V_{DD} – V_{EE}) p–p f_{in} = 4.5 MHz — MC14051B f_{in} = 30 MHz — MC14052B f_{in} = 55 MHz — MC14053B	—	10	– 50	—	dB
Channel Separation (Figure 8) (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD}–V_{EE}) p–p, f_{in} = 3.0 MHz	—	10	– 50	—	dB
Crosstalk, Control Input to Common O/I (Figure 9) (R_1 = 1 kΩ, R_L = 10 kΩ Control t_{TLH} = t_{THL} = 20 ns, Inhibit = V_{SS})	—	10	75	—	mV

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not lo be used for design purposes but In intended as an indication of the IC's potential performance.

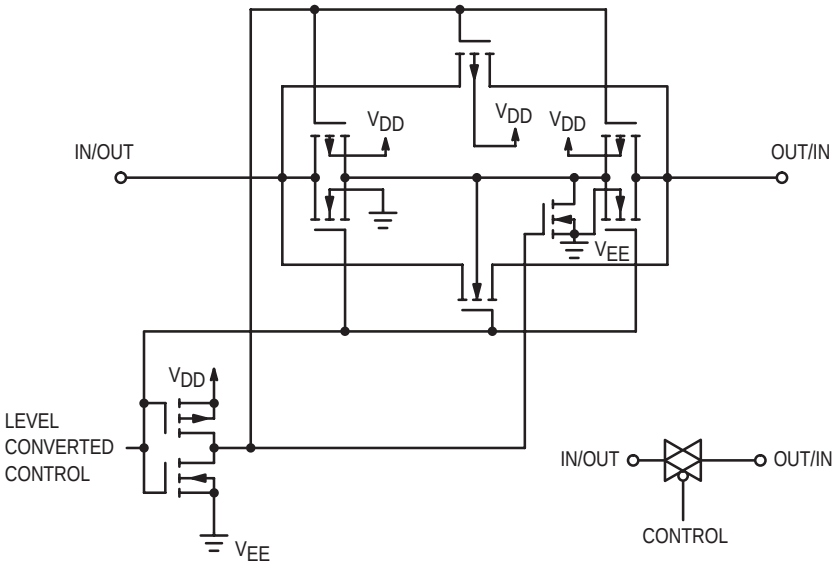


Figure 1. Switch Circuit Schematic

TRUTH TABLE

Control Inputs				ON Switches					
Inhibit	Select C*	B	A	MC14051B	MC14052B		MC14053B		
0	0	0	0	X0	Y0	X0	Z0	Y0	X0
0	0	0	1	X1	Y1	X1	Z0	Y0	X1
0	0	1	0	X2	Y2	X2	Z0	Y1	X0
0	0	1	1	X3	Y3	X3	Z0	Y1	X1
0	1	0	0	X4			Z1	Y0	X0
0	1	0	1	X5			Z1	Y0	X1
0	1	1	0	X6			Z1	Y1	X0
0	1	1	1	X7			Z1	Y1	X1
1	x	x	x	None	None		None		

*Not applicable for MC14052
x = Don't Care

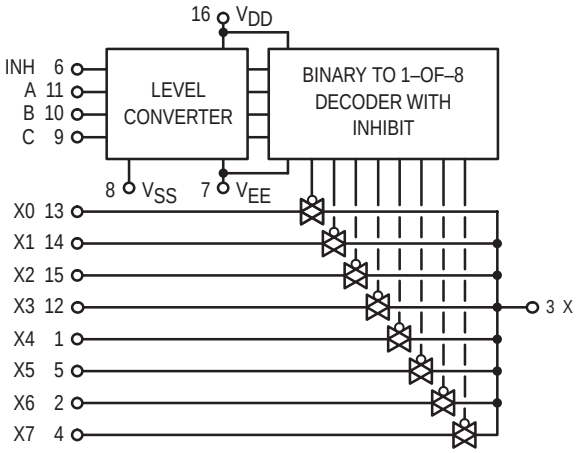


Figure 2. MC14051B Functional Diagram

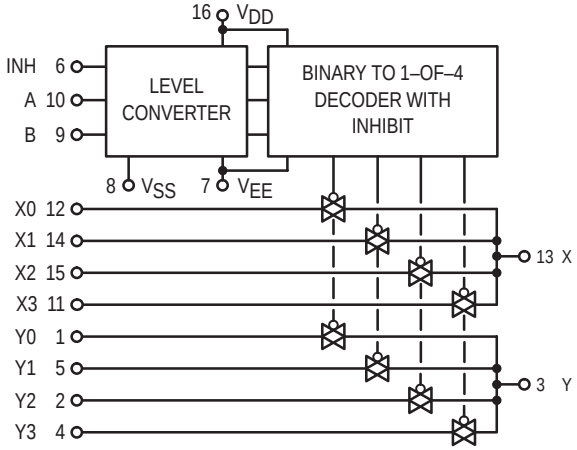


Figure 3. MC14052B Functional Diagram

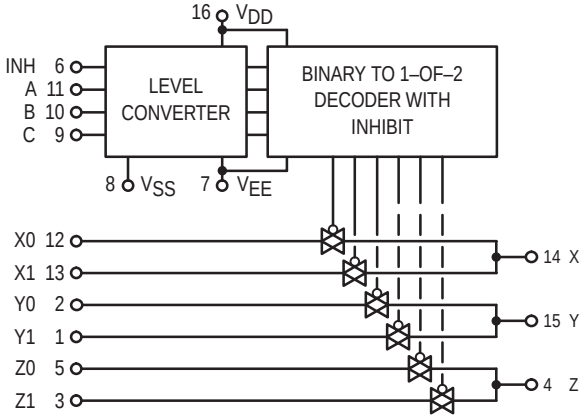


Figure 4. MC14053B Functional Diagram

TEST CIRCUITS

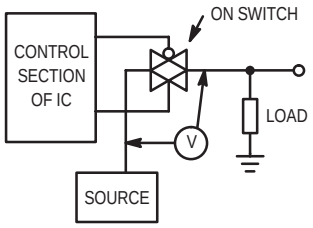


Figure 5. ΔV Across Switch

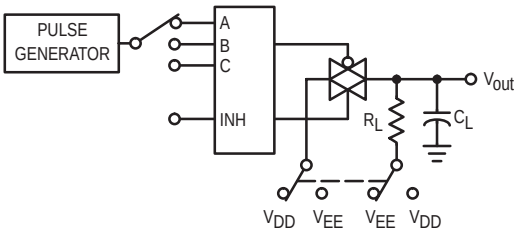


Figure 6. Propagation Delay Times, Control and Inhibit to Output

A, B, and C inputs used to turn ON or OFF
the switch under test.

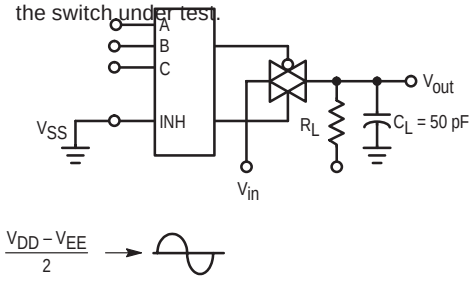


Figure 7. Bandwidth and Off–Channel Feedthrough Attenuation

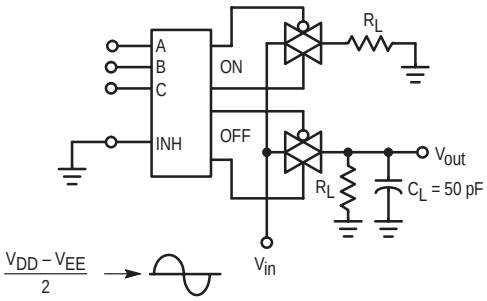


Figure 8. Channel Separation (Adjacent Channels Used For Setup)

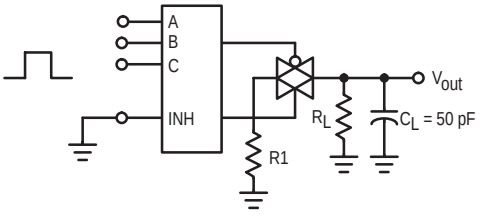


Figure 9. Crosstalk, Control Input to Common O/I

NOTE: See also Figures 7 and 8 in the MC14016B data sheet.

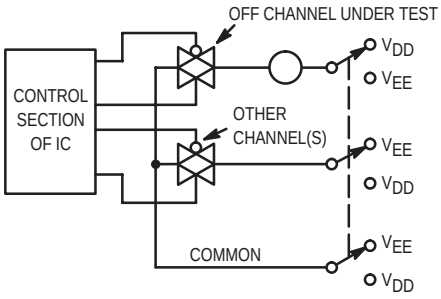


Figure 10. Off Channel Leakage

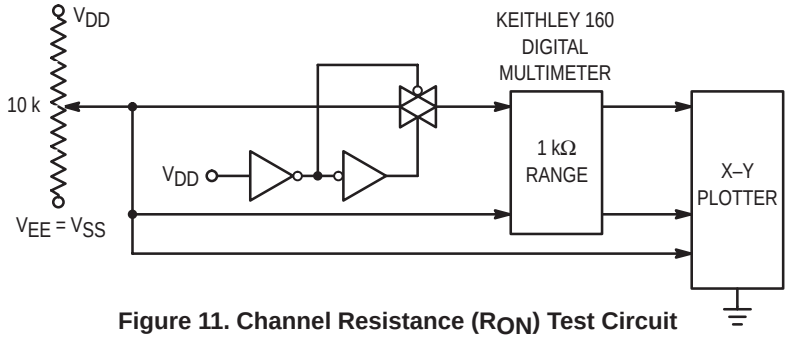


Figure 11. Channel Resistance (R_{ON}) Test Circuit

TYPICAL RESISTANCE CHARACTERISTICS

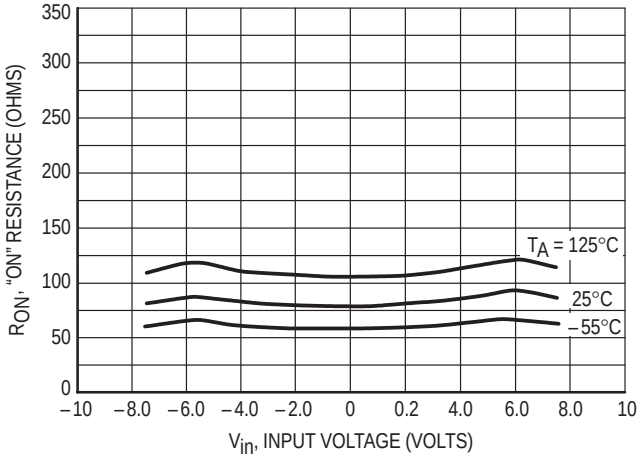


Figure 12. V_{DD} = 7.5 V, V_{EE} = – 7.5 V

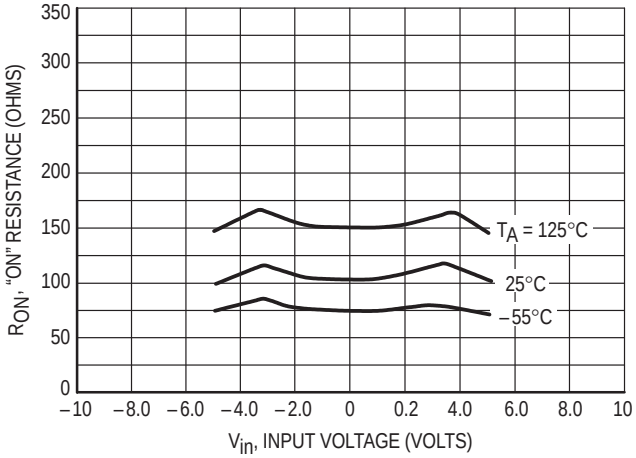


Figure 13. V_{DD} = 5.0 V, V_{EE} = – 5.0 V

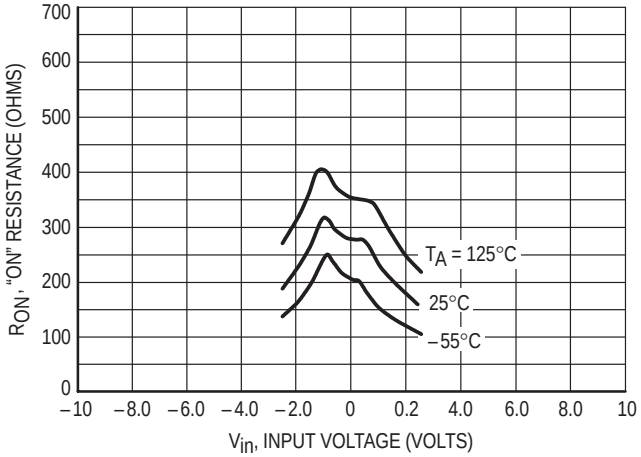


Figure 14. V_{DD} = 2.5 V, V_{EE} = – 2.5 V

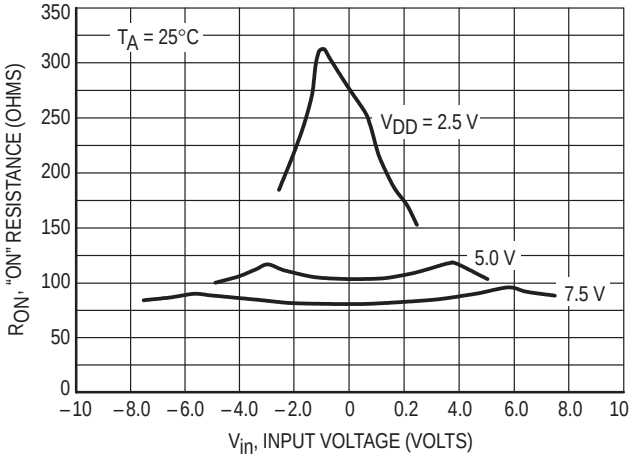


Figure 15. Comparison at 25°C, V_{DD} = –V_{EE}

APPLICATIONS INFORMATION

Figure A illustrates use of the on–chip level converter detailed in Figures 2, 3, and 4. The 0–to–5 V Digital Control signal is used to directly control a 9 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = + 5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{EE}. The V_{DD} voltage determines the maximum recommended peak above V_{SS}. The V_{EE} voltage determines the maximum swing below V_{SS}. For the example, $V_{DD} - V_{SS}$ = 5 V maximum swing above V_{SS}; $V_{SS} - V_{EE}$ = 5 V maximum swing below V_{SS}. The example shows a ± 4.5 V signal which allows a 1/2 volt margin at each peak. If voltage transients above V_{DD} and/or below V_{EE} are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{EE} is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{EE}.

Balanced supplies are not required. However, V_{SS} must be greater than or equal to V_{EE}. For example, V_{DD} = + 10 V, V_{SS} = + 5 V, and V_{EE} – 3 V is acceptable. See the Table below.

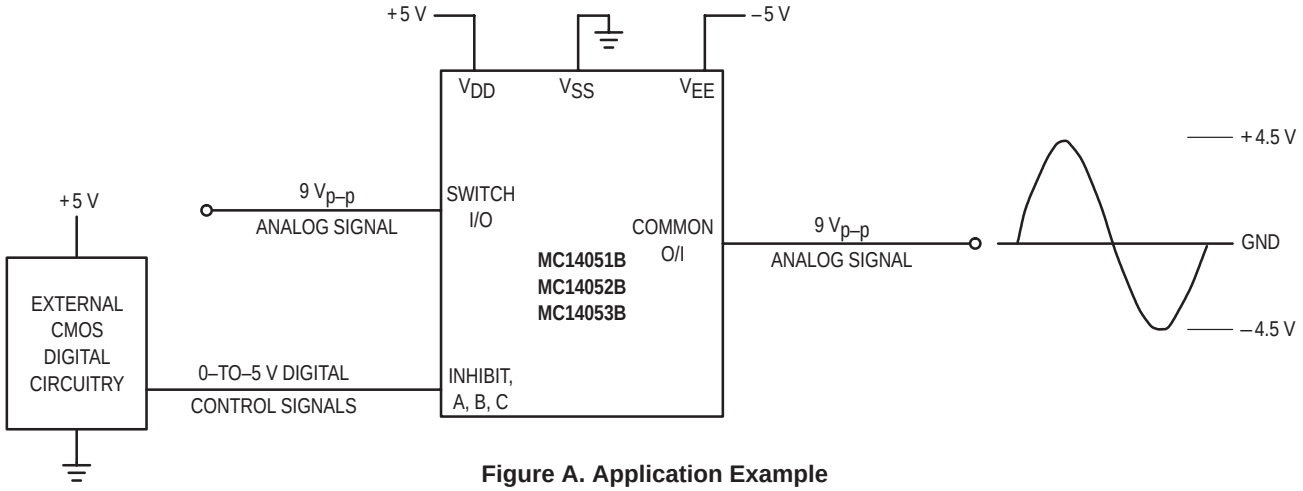


Figure A. Application Example

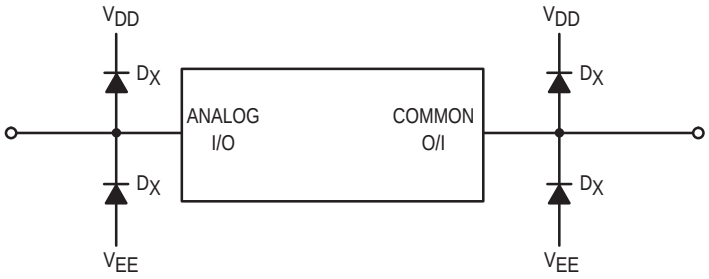


Figure B. External Germanium or Schottky Clipping Diodes

POSSIBLE SUPPLY CONNECTIONS

V_{DD} In Volts	V_{SS} In Volts	V_{EE} In Volts	Control Inputs Logic High/Logic Low In Volts	Maximum Analog Signal Range In Volts
+ 8	0	– 8	+ 8/0	+ 8 to – 8 = 16 V_{p-p}
+ 5	0	– 12	+ 5/0	+ 5 to – 12 = 17 V_{p-p}
+ 5	0	0	+ 5/0	+ 5 to 0 = 5 V_{p-p}
+ 5	0	– 5	+ 5/0	+ 5 to – 5 = 10 V_{p-p}
+ 10	+ 5	– 5	+ 10/ + 5	+ 10 to – 5 = 15 V_{p-p}

ORDERING & SHIPPING INFORMATION:

Device	Package	Shipping
MC14051BCP	PDIP–16	2000 Units per Box
MC14051BD	SOIC–16	48 Units per Rail
MC14051BDR2	SOIC–16	2500 Units / Tape & Reel
MC14051BDT	TSSOP–16	96 Units per Rail
MC14051BDTEL	TSSOP–16	2000 Units / Tape & Reel
MC14051BDTR2	TSSOP–16	2500 Units / Tape & Reel
MC14051BF	SOEIAJ–16	See Note 7.
MC14051BFEL	SOEIAJ–16	See Note 7.
MC14052BCP	PDIP–16	2000 Units per Box
MC14052BD	SOIC–16	48 Units per Rail
MC14052BDR2	SOIC–16	2500 Units / Tape & Reel
MC14052BDT	TSSOP–16	96 Units per Rail
MC14052BDTR2	TSSOP–16	2500 Units / Tape & Reel
MC14052BF	SOEIAJ–16	See Note 7.
MC14052BFEL	SOEIAJ–16	See Note 7.

ORDERING & SHIPPING INFORMATION:

MC14053BCP	PDIP–16	2000 Units per Box
MC14053BD	SOIC–16	48 Units per Rail
MC14053BDR2	SOIC–16	2500 Units / Tape & Reel
MC14053BDT	TSSOP–16	96 Units per Rail
MC14053BDTEL	TSSOP–16	2000 Units / Tape & Reel
MC14053BDTR2	TSSOP–16	2500 Units / Tape & Reel
MC14053BF	SOEIAJ–16	See Note 7.
MC14053BFEL	SOEIAJ–16	See Note 7.

7. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

MC14066B

Quad Analog Switch/Quad Multiplexer

The MC14066B consists of four independent switches capable of controlling either digital or analog signals. This quad bilateral switch is useful in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

The MC14066B is designed to be pin–for–pin compatible with the MC14016B, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

- Triple Diode Protection on All Control Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise — 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1.0 kHz typical
- Pin–for–Pin Replacement for CD4016, CD4016, MC14016B
- For Lower R_{ON}, Use The HC4066 High–Speed CMOS Device

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	–0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	–0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient) per Control Pin	±10	mA
I_{SW}	Switch Through Current	±25	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	–55 to +125	°C
T_{stg}	Storage Temperature Range	–65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ON Semiconductor

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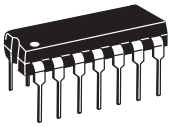
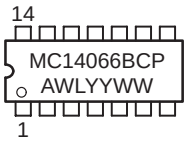
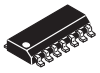
MARKING DIAGRAMS

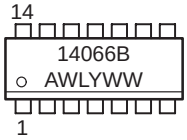


PDIP–14
P SUFFIX
CASE 646

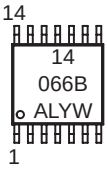


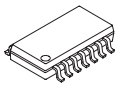


SOIC–14
D SUFFIX
CASE 751A



TSSOP–14
DT SUFFIX
CASE 948G





SOEIAJ–14
F SUFFIX
CASE 965

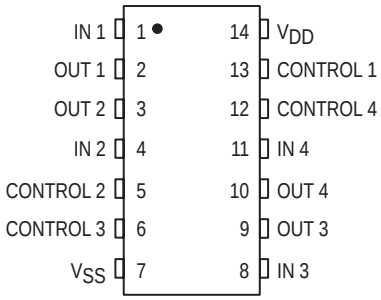
A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

ORDERING INFORMATION

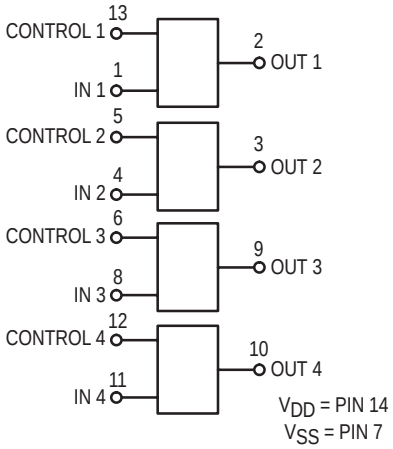
Device	Package	Shipping
MC14066BCP	PDIP–14	2000/Box
MC14066BD	SOIC–14	55/Rail
MC14066BDR2	SOIC–14	2500/Tape & Reel
MC14066BDT	TSSOP–14	96/Rail
MC14066BDTEL	TSSOP–14	2000/Tape & Reel
MC14066BDTR2	TSSOP–14	2500/Tape & Reel
MC14066BF	SOEIAJ–14	See Note 1.
MC14066BFEL	SOEIAJ–14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT

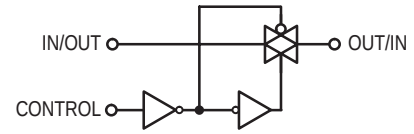


BLOCK DIAGRAM



LOGIC DIAGRAM AND TRUTH TABLE

(1/4 OF DEVICE SHOWN)



Control	Switch
0 = V_{SS}	OFF
1 = V_{DD}	ON

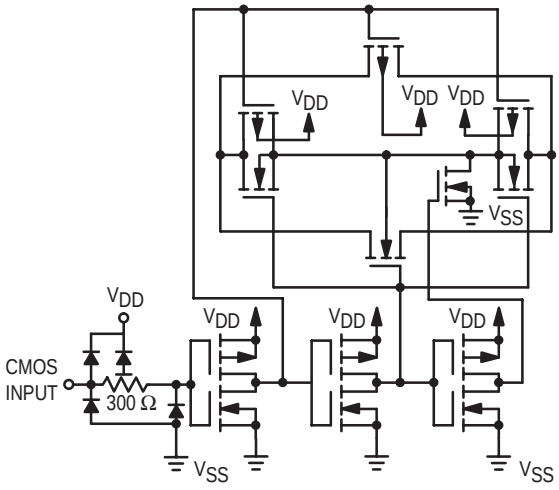
Logic Diagram Restrictions

$V_{SS} \le V_{in} \le V_{DD}$

$V_{SS} \le V_{out} \le V_{DD}$

CIRCUIT SCHEMATIC

(1/4 OF CIRCUIT SHOWN)



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	V_{DD}	—		3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I_{DD}	5.0 10 15	Control Inputs: $V_{in} = V_{SS}$ or V_{DD}, Switch I/O: $V_{SS} \le V_{I/O} \le V_{DD}$, and $\Delta V_{switch} \le 500$ mV (5.)	— — —	0.25 0.5 1.0	— — —	0.005 0.010 0.015	0.25 0.5 1.0	— — —	7.5 15 30	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package	$I_{D(AV)}$	5.0 10 15	T_A = 25°C only The channel component, $(V_{in} - V_{out})/R_{on}$, is not included.)	Typical			(0.07 μA/kHz) f + I_{DD} (0.20 μA/kHz) f + I_{DD} (0.36 μA/kHz) f + I_{DD}				μA
CONTROL INPUTS (Voltages Referenced to V_{SS})											
Low–Level Input Voltage	V_{IL}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High–Level Input Voltage	V_{IH}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I_{in}	15	V_{in} = 0 or V_{DD}	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	μA
Input Capacitance	C_{in}	—		—	—	—	5.0	7.5	—	—	pF
SWITCHES IN AND OUT (Voltages Referenced to V_{SS})											
Recommended Peak–to–Peak Voltage Into or Out of the Switch	$V_{I/O}$	—	Channel On or Off	0	V_{DD}	0	—	V_{DD}	0	V_{DD}	V_{p-p}
Recommended Static or Dynamic Voltage Across the Switch (5.) (Figure 1)	ΔV_{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V_{OO}	—	V_{in} = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R_{on}	5.0 10 15	$\Delta V_{switch} \le 500$ mV (5.), $V_{in} = V_{IL}$ or V_{IH} (Control), and V_{in} = 0 to V_{DD} (Switch)	— — —	800 400 220	— — —	250 120 80	1050 500 280	— — —	1200 520 300	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5.0 10 15		— — —	70 50 45	— — —	25 10 10	70 50 45	— — —	135 95 65	Ω
Off–Channel Leakage Current (Figure 6)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	± 0.05	±100	—	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	—	Switch Off	—	—	—	10	15	—	—	pF
Capacitance, Feedthrough (Switch Off)	$C_{I/O}$	— —		—	—	—	0.47	—	—	—	pF

4. Data labeled “Typ” is not to be used for design purposes, but is intended as an indication of the IC’s potential performance.
5. For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS (6.) (C_L = 50 pF, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (7.)	Max	Unit
Propagation Delay Times V_{SS} = 0 Vdc	t_{PLH},t_{PHL}					ns
Input to Output (R_L = 10 kΩ)						
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 15.5 ns		5.0	—	20	40	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 6.0 ns		10	—	10	20	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 4.0 ns		15	—	7.0	15	
Control to Output (R_L = 1 kΩ) (Figure 2)	t_{PHZ}					ns
Output “1” to High Impedance		5.0	—	40	80	
		10	—	35	70	
		15	—	30	60	
Output “0” to High Impedance	t_{PLZ}	5.0	—	40	80	ns
		10	—	35	70	
		15	—	30	60	
High Impedance to Output “1”	t_{PZH}	5.0	—	60	120	ns
		10	—	20	40	
		15	—	15	30	
High Impedance to Output “0”	t_{PZL}	5.0	—	60	120	ns
		10	—	20	40	
		15	—	15	30	
Second Harmonic Distortion V_{SS} = – 5 Vdc (V_{in} = 1.77 Vdc, RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	—	5.0	—	0.1	—	%
Bandwidth (Switch ON) (Figure 3) V_{SS} = – 5 Vdc (R_L = 1 kΩ, 20 Log (V_{out}/V_{in}) = – 3 dB, C_L = 50 pF, V_{in} = 5 $V_{p–p}$)	—	5.0	—	65	—	MHz
Feedthrough Attenuation (Switch OFF) V_{SS} = – 5 Vdc (V_{in} = 5 $V_{p–p}$, R_L = 1 kΩ, f_{in} = 1.0 MHz) (Figure 3)	—	5.0	—	– 50	—	dB
Channel Separation (Figure 4) V_{SS} = – 5 Vdc (V_{in} = 5 $V_{p–p}$, R_L = 1 kΩ, f_{in} = 8.0 MHz) (Switch A ON, Switch B OFF)	—	5.0	—	– 50	—	dB
Crosstalk, Control Input to Signal Output (Figure 5) V_{SS} = – 5 Vdc (R_1 = 1 kΩ, R_L = 10 kΩ, Control t_{TLH} = t_{THL} = 20 ns)	—	5.0	—	300	—	$mV_{p–p}$

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

TEST CIRCUITS

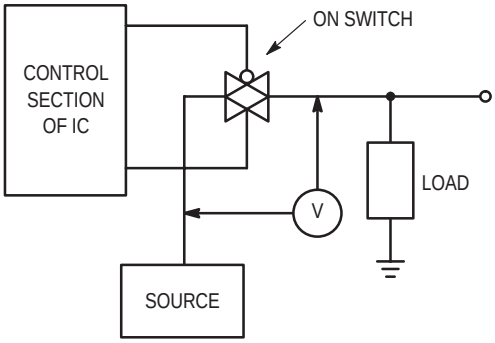


Figure 1. ΔV Across Switch

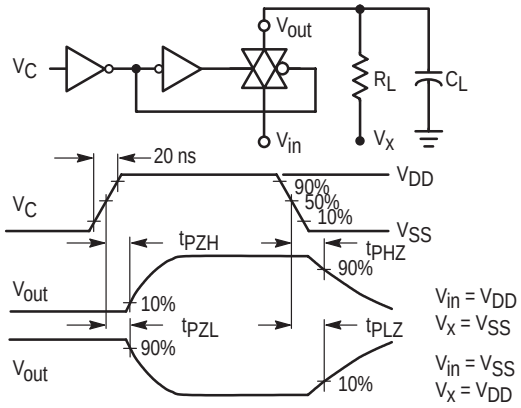


Figure 2. Turn–On Delay Time Test Circuit and Waveforms

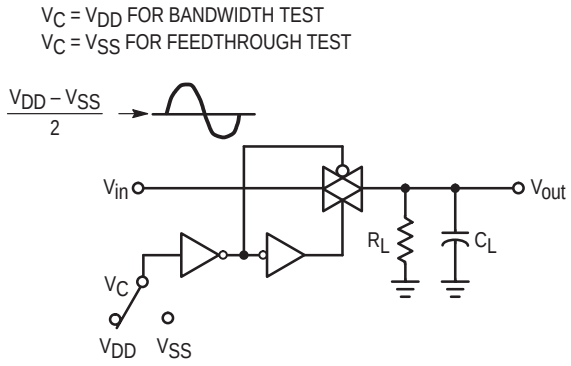


Figure 3. Bandwidth and Feedthrough Attenuation

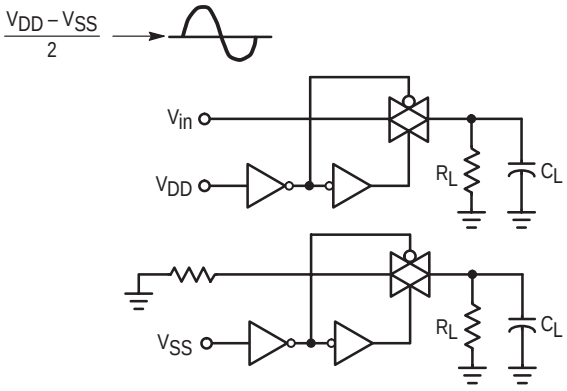


Figure 4. Channel Separation

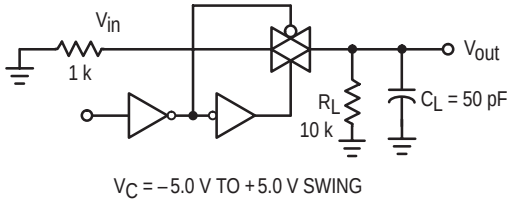


Figure 5. Crosstalk, Control to Output

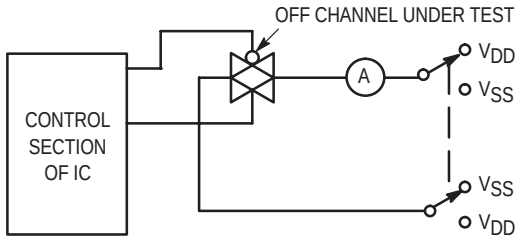


Figure 6. Off Channel Leakage

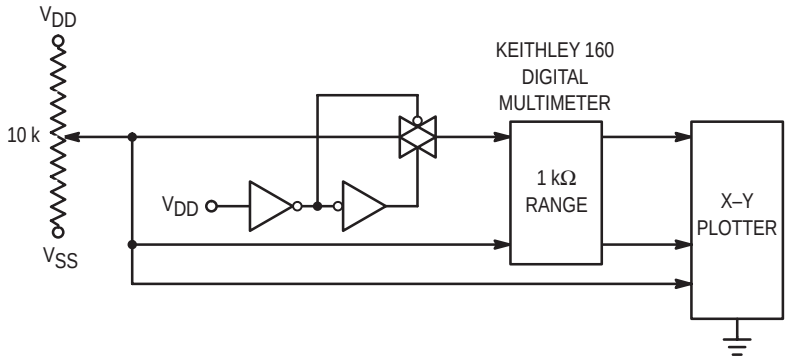


Figure 7. Channel Resistance (R_{ON}) Test Circuit

TYPICAL RESISTANCE CHARACTERISTICS

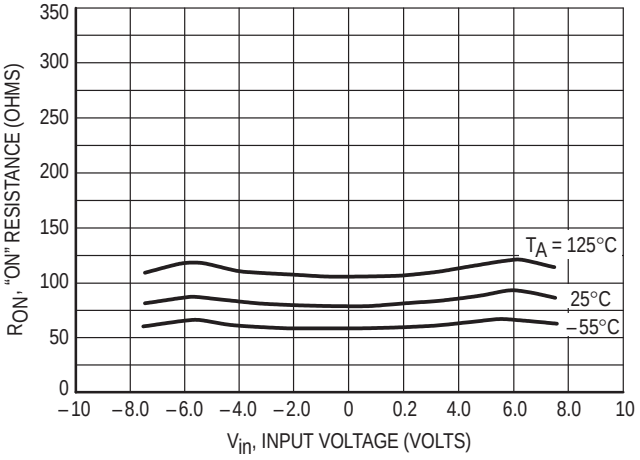


Figure 8. V_{DD} = 7.5 V, V_{SS} = – 7.5 V

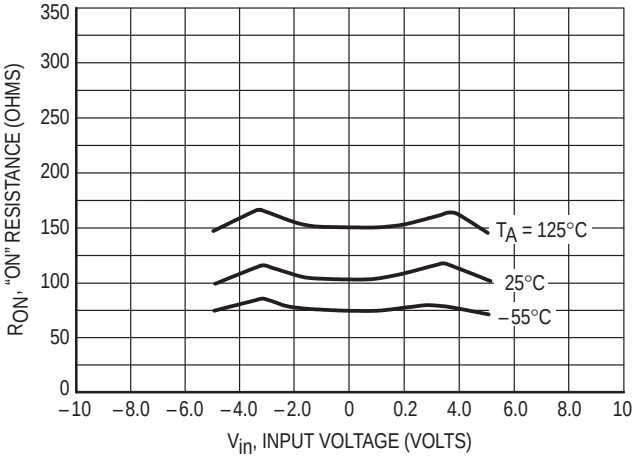


Figure 9. V_{DD} = 5.0 V, V_{SS} = – 5.0 V

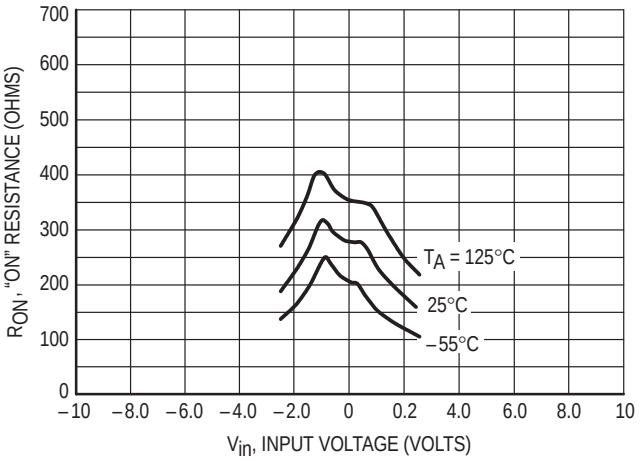


Figure 10. V_{DD} = 2.5 V, V_{SS} = – 2.5 V

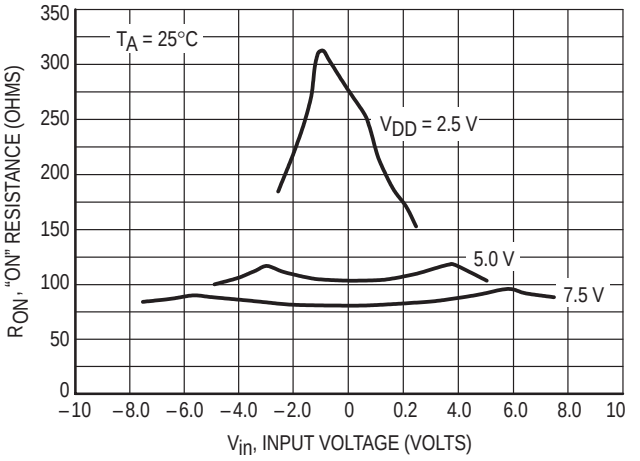


Figure 11. Comparison at 25°C, V_{DD} = –V_{SS}

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0–to–5 volt digital control signal is used to directly control a 5 volt peak–to–peak analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage, the V_{SS} voltage is logic low. For the example, V_{DD} = + 5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS}. The analog voltage must not swing higher than V_{DD} or lower than V_{SS}.

The example shows a 5 volt peak–to–peak signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_X) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{SS} is 18.0 volts. Most parameters are specified up to 15 volts which is the *recommended* maximum difference between V_{DD} and V_{SS}.

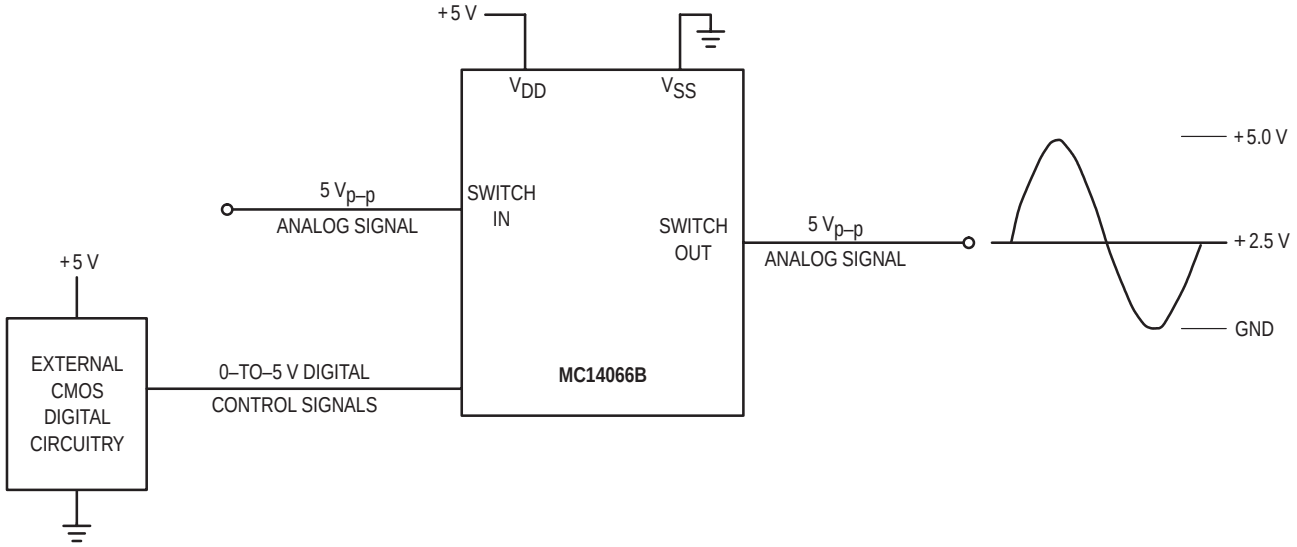


Figure A. Application Example

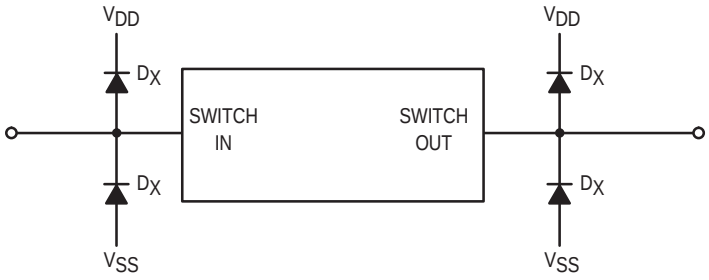


Figure B. External Germanium or Schottky Clipping Diodes

MC14067B

Analog Multiplexers / Demultiplexers

The MC14067 multiplexer/demultiplexer is a digitally controlled analog switch featuring low ON resistance and very low leakage current. This device can be used in either digital or analog applications.

The MC14067 is a 16–channel multiplexer/demultiplexer with an inhibit and four binary control inputs A, B, C, and D. These control inputs select 1–of–16 channels by turning ON the appropriate analog switch (see MC14067 truth table.)

- Low OFF Leakage Current
- Matched Channel Resistance
- Low Quiescent Power Consumption
- Low Crosstalk Between Channels
- Wide Operating Voltage Range: 3 to 18 V
- Low Noise
- Pin for Pin Replacement for CD4067B

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient), per Control Pin	± 10	mA
I_{sw}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Ambient Temperature Range	– 55 to + 125	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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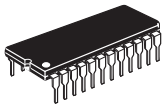
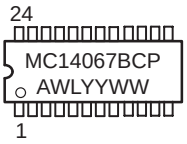
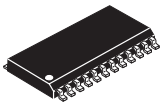
MARKING DIAGRAMS

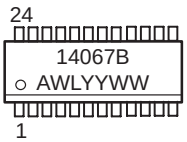


PDIP–24
P SUFFIX
CASE 709





SOIC–24
DW SUFFIX
CASE 751E



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

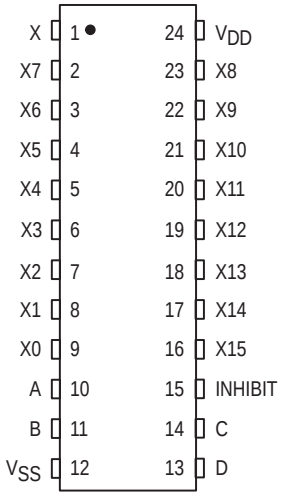
ORDERING INFORMATION

Device	Package	Shipping
MC14067BCP	PDIP–24	15/Rail
MC14067BDW	SOIC–24	30/Rail
MC14067BDWR2	SOIC–24	1000/Tape & Reel

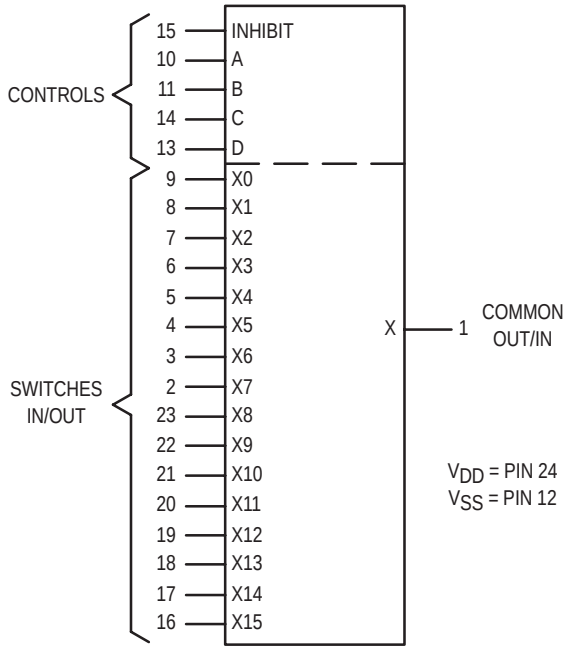
MC14067 TRUTH TABLE

Control Inputs					Selected Channel
A	B	C	D	Inh	
X	X	X	X	1	None
0	0	0	0	0	X0
1	0	0	0	0	X1
0	1	0	0	0	X2
1	1	0	0	0	X3
0	0	1	0	0	X4
1	0	1	0	0	X5
0	1	1	0	0	X6
1	1	1	0	0	X7
0	0	0	1	0	X8
1	0	0	1	0	X9
0	1	0	1	0	X10
1	1	0	1	0	X11
0	0	1	1	0	X12
1	0	1	1	0	X13
0	1	1	1	0	X14
1	1	1	1	0	X15

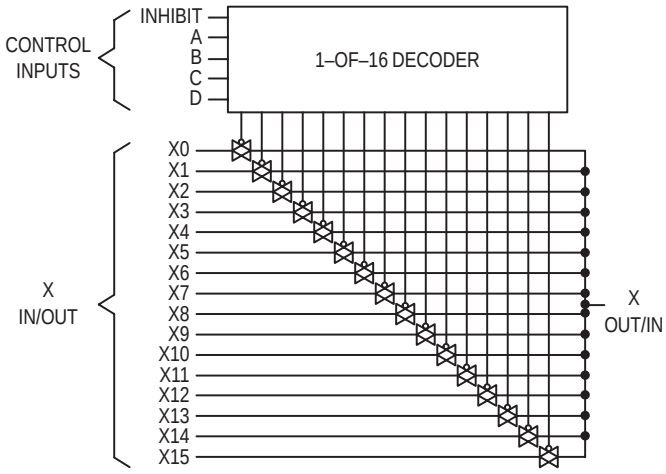
MC14067B
PIN ASSIGNMENT



MC14067B
16–Channel Analog
Multiplexer/Demultiplexer



MC14067 FUNCTIONAL DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (3.)	25°C Max	125°C Min	125°C Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{SS})											
Power Supply Voltage Range	V_{DD}	—		3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I_{DD}	5.0 10 15	Control Inputs: V_{in} = V_{SS} or V_{DD}, Switch I/O: $V_{SS} \le V_{I/O} \le V_{DD}$, and $\Delta V_{switch} \le 500\,mV$ (4.)	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package	$I_{D(AV)}$	5.0 10 15	T_A = 25°C only (The channel component, $(V_{in} - V_{out})/R_{on}$, is not included.)	Typical			(0.07 μA/kHz) f + I_{DD} (0.20 μA/kHz) f + I_{DD} (0.36 μA/kHz) f + I_{DD}				μA
CONTROL INPUTS — INHIBIT, A, B, C, D (Voltages Referenced to V_{SS})											
Low–Level Input Voltage	V_{IL}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High–Level Input Voltage	V_{IH}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I_{in}	15	V_{in} = 0 or V_{DD}	—	± 0.1	—	±0.00001	± 0.1	—	1.0	μA
Input Capacitance	C_{in}	—		—	—	—	5.0	7.5	—	—	pF
SWITCHES IN/OUT AND COMMONS OUT/IN — X, Y (Voltages Referenced to V_{SS})											
Recommended Peak–to–Peak Voltage Into or Out of the Switch	$V_{I/O}$	—	Channel On or Off	0	V_{DD}	0	—	V_{DD}	0	V_{DD}	V_{p-p}
Recommended Static or Dynamic Voltage Across the Switch (4.) (Figure 1)	ΔV_{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V_{OO}	—	V_{in} = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R_{on}	5.0 10 15	$\Delta V_{switch} \le 500$ mV (4.), $V_{in} = V_{IL}$ or V_{IH} (Control), and V_{in} 0 to V_{DD} (Switch)	— — —	800 400 220	— — —	250 120 80	1050 500 280	— — —	1300 550 320	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5.0 10 15		— — —	70 50 45	— — —	25 10 10	70 50 45	— — —	135 95 65	Ω
Off–Channel Leakage Current (Figure 2)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	± 100	—	± 0.05	±100	—	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	—	Inhibit = V_{DD}	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	$C_{O/I}$	—	Inhibit = V_{DD} (MC14067B) (MC14097B)	— —	— —	— —	100 60	— —	— —	— —	pF
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	— —	Pins Not Adjacent Pins Adjacent	—	—	—	0.47	—	—	—	pF

3. Data labeled “Typ” is not to be used for design purposes, but is intended as an indication of the IC’s potential performance.
4. For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	$V_{DD} - V_{SS}$ Vdc	Typ (5.)	Max	Unit
Propagation Delay Times Channel Input–to–Channel Output (R_L = 200 kΩ) MC14067B	t_{PLH}, t_{PHL} (Figure 3)	5.0 10 15	35 15 12	90 40 30	ns
Control Input–to–Channel Output Channel Turn–On Time (R_L = 10 kΩ) MC14067B	t_{PZH}, t_{PZL} (Figure 4)	5.0 10 15	240 115 75	600 290 190	ns
Channel Turn–Off Time (R_L = 300 kΩ) MC14067B	t_{PHZ}, t_{PLZ} (Figure 4)	5.0 10 15	250 120 75	625 300 190	ns
Any Pair of Address Inputs to Output MC14067B	t_{PLH}, t_{PHL}	5.0 10 15	280 115 85	700 290 215	ns
Second Harmonic Distortion (R_L = 10 kΩ, f = 1 kHz, V_{in} = 5 $V_{p–p}$)	—	10	0.3	—	%
ON Channel Bandwidth [R_L = 1 kΩ, V_{in} = 1/2 (V_{DD} – V_{SS}) $_{p–p}$(sine–wave)] 20 Log10 (V_{out}/V_{in}) = – 3 dB MC14067B	BW (Figure 5)	10	15	—	MHz
Off Channel Feedthrough Attenuation [R_L = 1 kΩ, V_{in} = 1/2 (V_{DD}–V_{SS}) $_{p–p}$(sine–wave)] f_{in} = 20 MHz – MC14067B	— (Figure 5)	10	– 40	—	dB
Channel Separation [R_L = 1 kΩ, V_{in} = 1/2 (V_{DD}–V_{SS}) $_{p–p}$ (sine–wave)] f_{in} = 20 MHz	— (Figure 6)	10	– 40	—	dB
Crosstalk, Control Inputs–to–Common O/I (R1 = 1 kΩ, R_L = 10 kΩ, Control t_r = t_f = 20 ns, Inhibit = V_{SS})	— (Figure 7)	10	30	—	mV

5. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

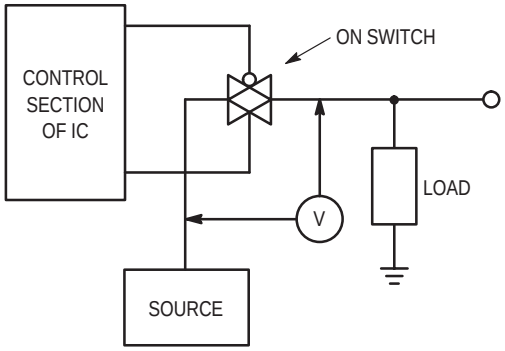


Figure 1. ΔV Across Switch

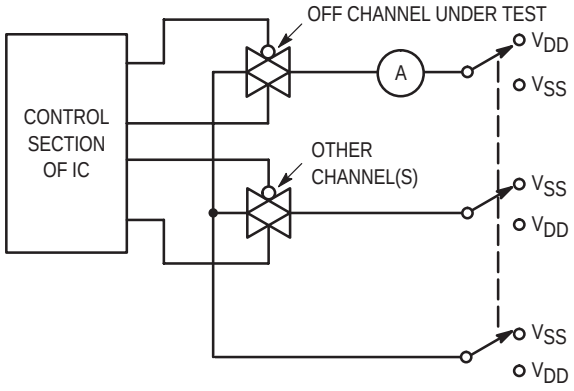


Figure 2. Off Channel Leakage

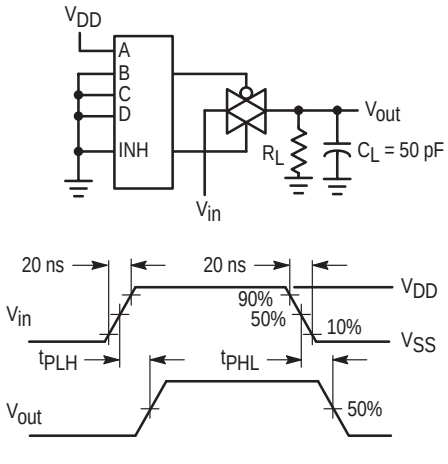


Figure 3. Propagation Delay Test Circuit and Waveforms V_{in} to V_{out}

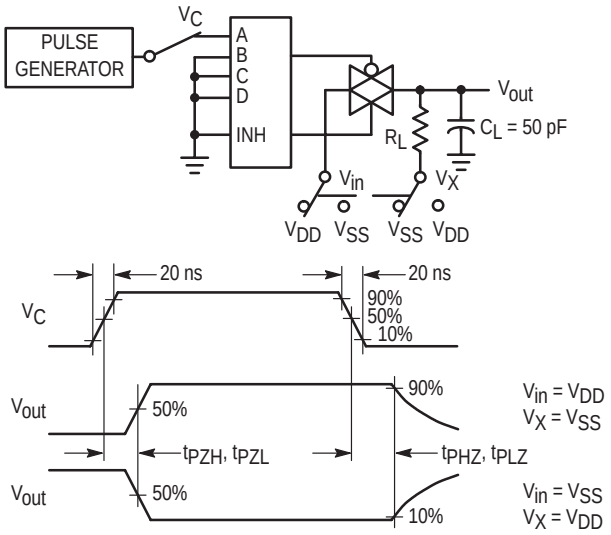


Figure 4. Turn–On and Delay Turn–Off Test Circuit and Waveforms

A, B, and C inputs used to turn ON or OFF the switch under test.

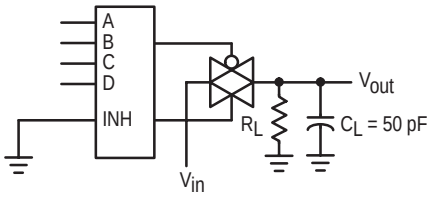


Figure 5. Bandwidth and Off–Channel Feedthrough Attenuation

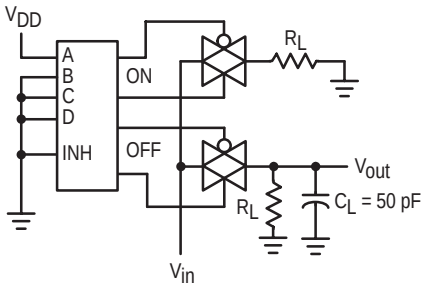


Figure 6. Channel Separation (Adjacent Channels Used for Setup)

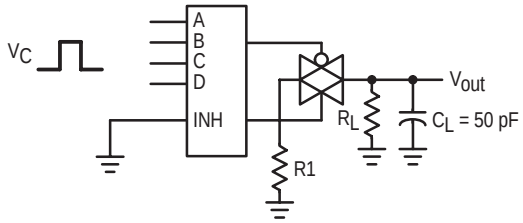


Figure 7. Crosstalk, Control to Common O/I

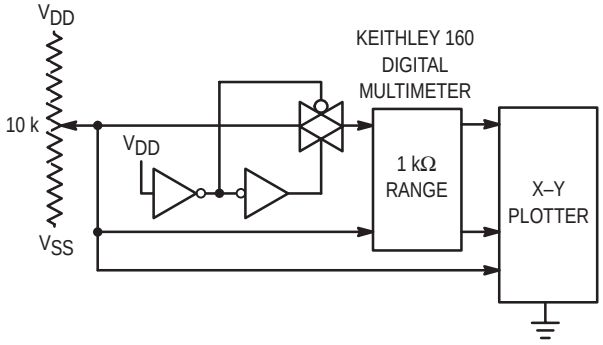


Figure 8. Channel Resistance (R_{ON}) Test Circuit

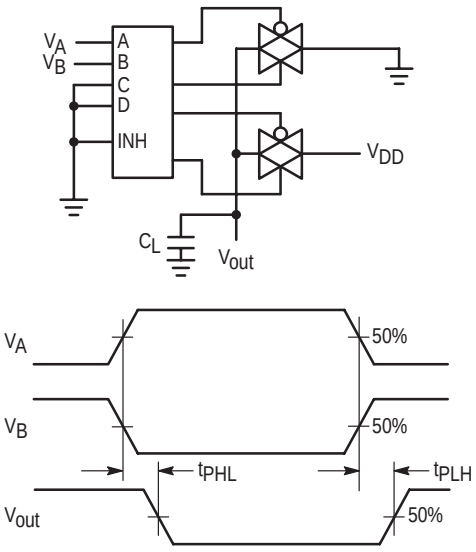


Figure 9. Propagation Delay, Any Pair of Address Inputs to Output

TYPICAL RESISTANCE CHARACTERISTICS

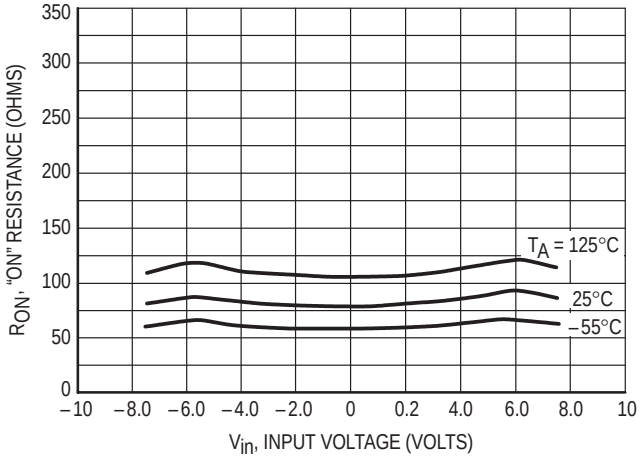


Figure 10. V_{DD} = 7.5 V, V_{SS} = – 7.5 V

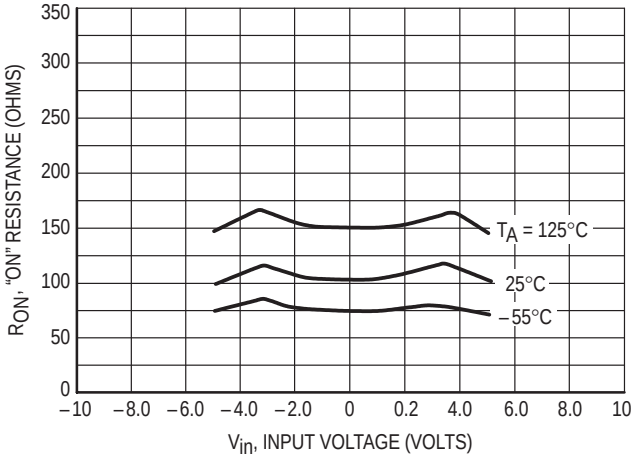


Figure 11. V_{DD} = 5.0 V, V_{SS} = – 5.0 V

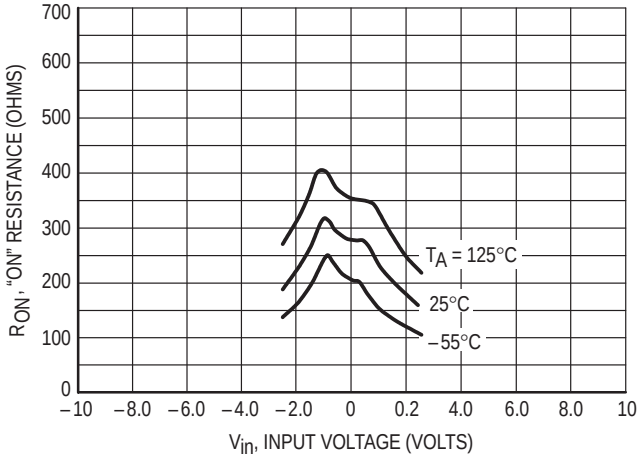


Figure 12. V_{DD} = 2.5 V, V_{SS} = – 2.5 V

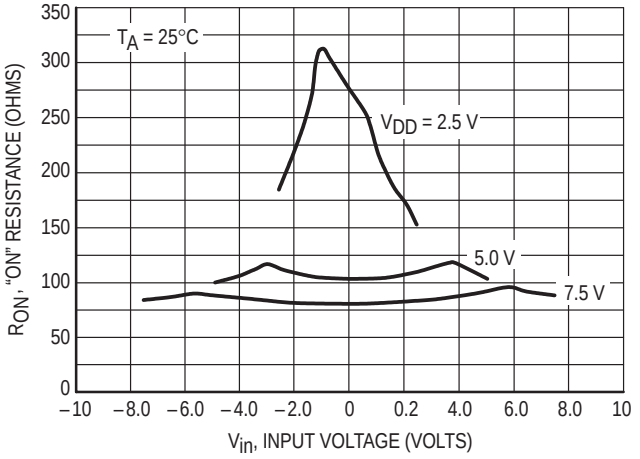


Figure 13. Comparison at 25°C, $V_{DD} = -V_{SS}$

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Multiplexer/Demultiplexer. The 0–to–5 volt Digital Control signal is used to directly control a 5 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example. V_{DD} = + 5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS}. The analog voltage must swing neither higher than V_{DD} nor lower than V_{SS}. The example shows a 5 V_{p-p} signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_X) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between V_{DD} and V_{SS} is 18.0 volts. Most parameters are specified up to 15 V which is the recommended maximum difference between V_{DD} and V_{SS}.

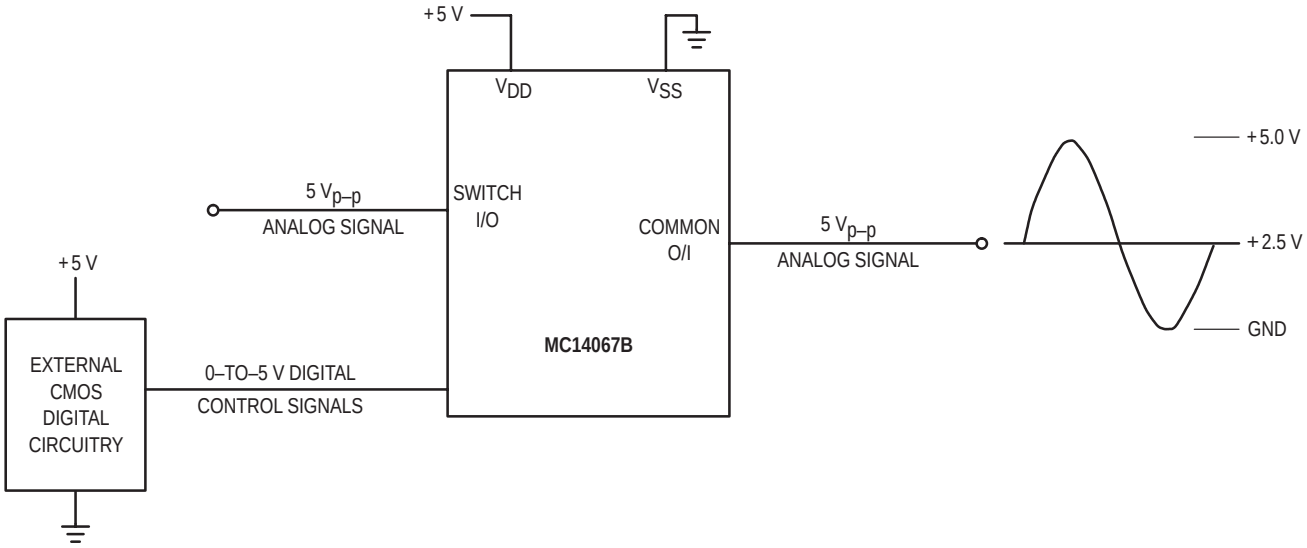


Figure A. Application Example

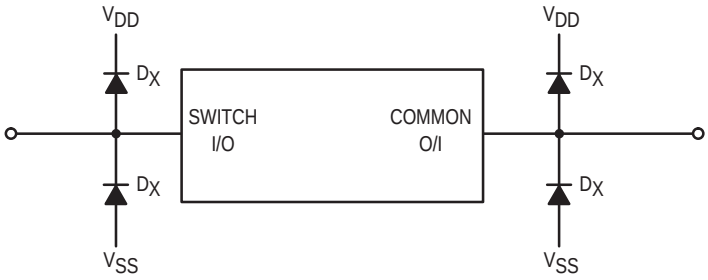


Figure B. External Germanium or Schottky Clipping Diodes

MC14512B

8-Channel Data Selector

The MC14512B is an 8–channel data selector constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequence generation.

- Diode Protection on All Inputs
- Single Supply Operation
- 3–State Output (Logic “1”, Logic “0”, High Impedance)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range

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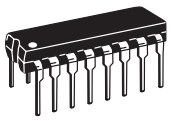
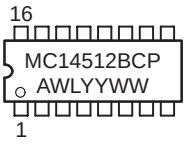
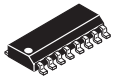
MARKING DIAGRAMS

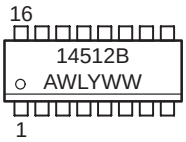


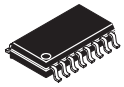
PDIP–16
P SUFFIX
CASE 648



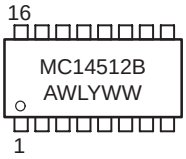


SOIC–16
D SUFFIX
CASE 751B





SOEIAJ–16
F SUFFIX
CASE 966



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note NO TAG)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	–0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	–0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note NO TAG)	500	mW
T_A	Ambient Temperature Range	–55 to +125	°C
T_{stg}	Storage Temperature Range	–65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ORDERING INFORMATION

Device	Package	Shipping
MC14512BCP	PDIP–16	2000/Box
MC14512BD	SOIC–16	48/Rail
MC14512BDR2	SOIC–16	2500/Tape & Reel
MC14512BF	SOEIAJ–16	See Note 1.
MC14512BFL1	SOEIAJ–16	See Note 1.
MC14512BFR1	SOEIAJ–16	See Note 1.
MC14512BFR2	SOEIAJ–16	See Note 1.

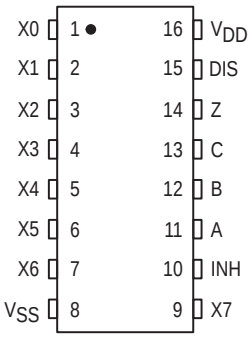
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

TRUTH TABLE

C	B	A	Inhibit	Disable	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
X	X	X	1	0	0
X	X	X	X	1	High Impedance

X = Don't Care

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
“1” Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage “0” Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
“1” Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	
(V_{OH} = 4.6 Vdc)		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
(V_{OH} = 9.5 Vdc)		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc)		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.8 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.6 µA/kHz) f + I_{DD}							
		15	I_T = (2.4 µA/kHz) f + I_{DD}							
Three–State Leakage Current	I_{TL}	15	—	± 0.1	—	± 0.0001	± 0.1	—	± 3.0	µAdc

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS [7.] (C_L = 50 pF, T_A = 25°C, See Figure 1)

Characteristic	Symbol	V_{DD}	All Types		Unit
			Typ [8.]	Max	
Output Rise and Fall Time	t_{TLH},				ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	40	80	
Propagation Delay Time (Figure 2)	t_{PLH}				ns
Inhibit, Control, or Data to Z		5.0	330	650	
		10	125	250	
		15	85	170	
Propagation Delay Time (Figure 2)	t_{PHL}				ns
Inhibit, Control, or Data to Z		5.0	330	650	
		10	125	250	
		15	85	170	
3–State Output Delay Times (Figure 3)	t_{PHZ}, t_{PLZ},	5.0	60	150	ns
“1” or “0” to High Z, and	t_{PZH}, t_{PZL}	10	35	100	
High Z to “1” or “0”		15	30	75	

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

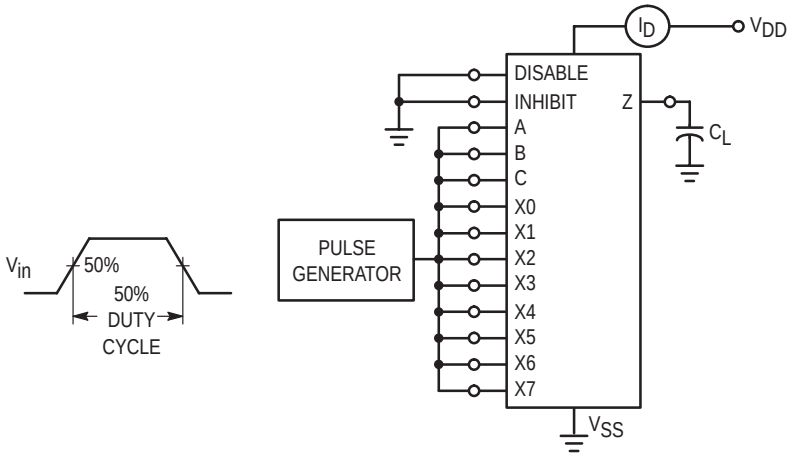
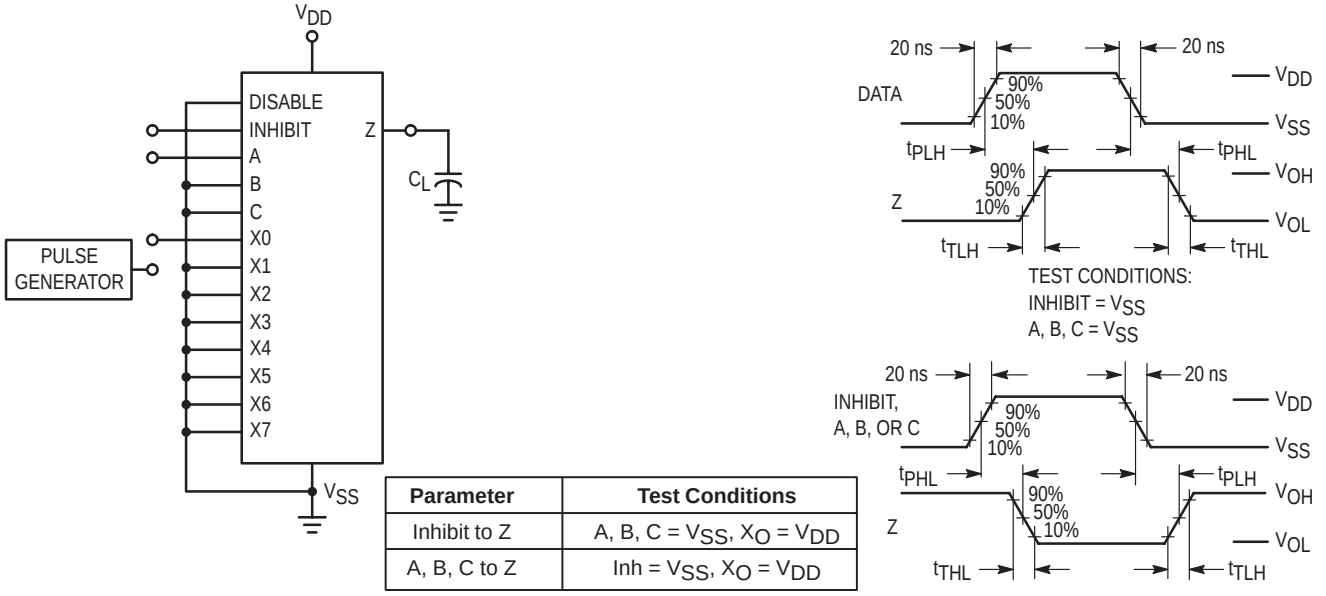
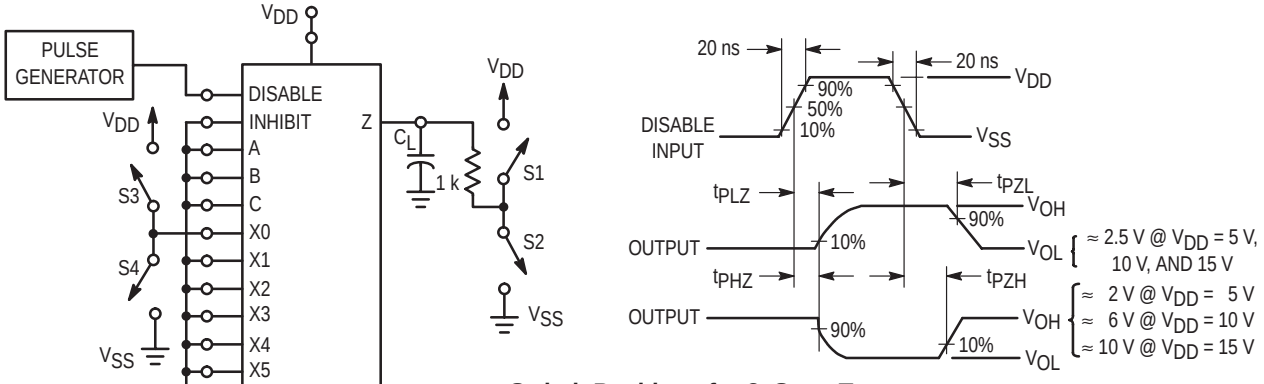


Figure 1. Power Dissipation Test Circuit and Waveform



Parameter	Test Conditions
Inhibit to Z	A, B, C = V_{SS}, X_O = V_{DD}
A, B, C to Z	Inh = V_{SS}, X_O = V_{DD}

Figure 2. AC Test Circuit and Waveforms

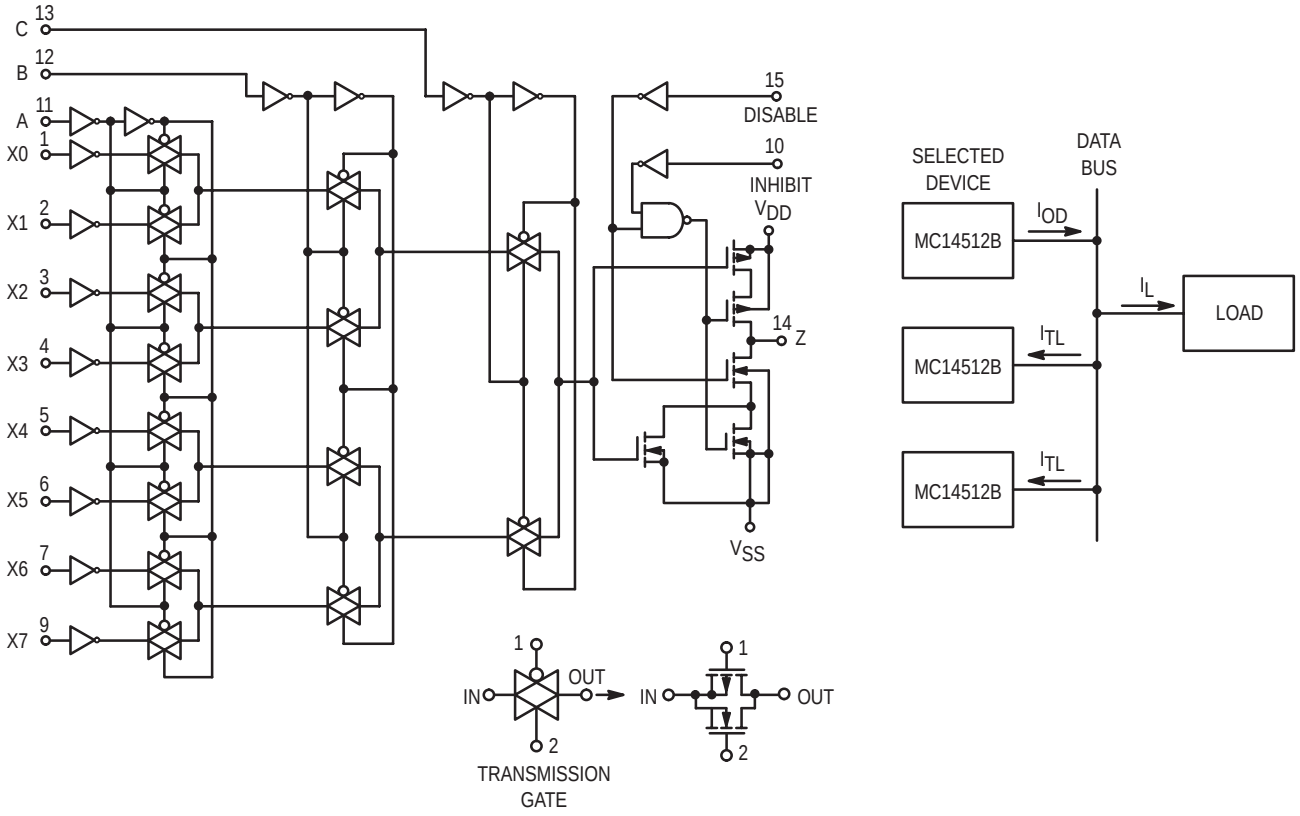


Switch Positions for 3–State Test

Test	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open

Figure 3. 3–State AC Test Circuit and Waveform

LOGIC DIAGRAM



3–STATE MODE OF OPERATION

Output terminals of several MC14512B 8–Bit Data Selectors can be connected to a single date bus as shown. One MC14512B is selected by the 3–state control, and the remaining devices are disabled into a high–impedance "off" state. The number of 8–bit data selectors, N, that may be connected to a bus line is determined from the output drive current, I_{OD}, 3–state or disable output leakage current, I_{TL}, and the load current, I_L, required to drive the bus line (including fanout to other device inputs), and can be calculated by:

$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic state of the bus line.

MC14551B

Quad 2-Channel Analog Multiplexer/Demultiplexer

The MC14551B is a digitally–controlled analog switch. This device implements a 4PDT solid state switch with low ON impedance and very low OFF Leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- Triple Diode Protection on All Control Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range ($V_{DD} – V_{EE}$) = 3.0 to 18 V
  Note: V_{EE} must be $\leq V_{SS}$
- Linearized Transfer Characteristics
- Low Noise — 12 $nV\sqrt{Cycle}$, f ≥ 1.0 kHz typical
- For Low R_{ON}, Use The HC4051, HC4052, or HC4053 High–Speed CMOS Devices
- Switch Function is Break Before Make

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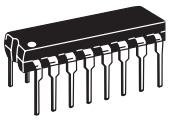
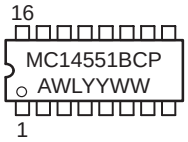
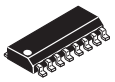
MARKING DIAGRAMS

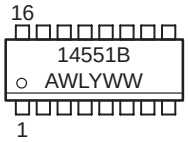


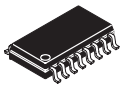
PDIP–16
P SUFFIX
CASE 648



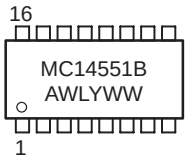


SOIC–16
D SUFFIX
CASE 751B





SOEIAJ–16
F SUFFIX
CASE 966



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

MAXIMUM RATINGS (2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range (Referenced to V_{EE}, $V_{SS} \geq V_{EE}$)	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient) (Referenced to V_{SS} for Control Input & V_{EE} for Switch I/O)	– 0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient), per Control Pin	± 10	mA
I_{sw}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package (3.)	500	mW
T_A	Ambient Temperature Range	– 55 to + 125	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$ for control inputs and $V_{EE} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$ for Switch I/O.

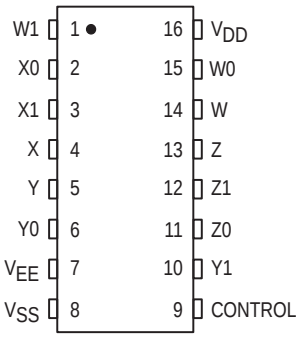
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS}, V_{EE} or V_{DD}). Unused outputs must be left open.

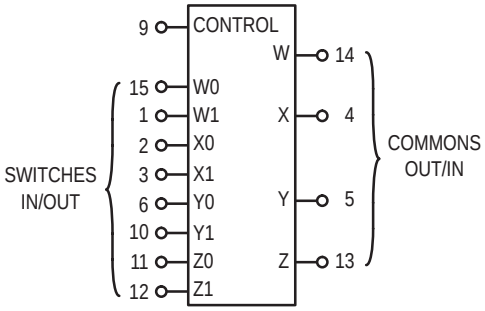
ORDERING INFORMATION

Device	Package	Shipping
MC14551BCP	PDIP–16	2000/Box
MC14551BD	SOIC–16	48/Rail
MC14551BDR2	SOIC–16	2500/Tape & Reel
MC14551BF	SOEIAJ–16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT





V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

Control	ON
0	W0 X0 Y0 Z0
1	W1 X1 Y1 Z1

NOTE: Control Input referenced to V_{SS}, Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be $\leq V_{SS}$.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	V_{DD}	—	$V_{DD} - 3.0 \geq V_{SS} \geq V_{EE}$	3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I_{DD}	5.0 10 15	Control Inputs: V_{in} = V_{SS} or V_{DD}, Switch I/O: $V_{EE} \leq V_{I/O} \leq V_{DD}$, and $\Delta V_{switch} \leq 500$ mV (5.)	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	$I_{D(AV)}$	5.0 10 15	T_A = 25°C only (The channel component, $(V_{in} - V_{out})/R_{on}$, is not included.)	Typical			(0.07 μA/kHz) f + I_{DD} (0.20 μA/kHz) f + I_{DD} (0.36 μA/kHz) f + I_{DD}				μA
CONTROL INPUT (Voltages Referenced to V_{SS})											
Low–Level Input Voltage	V_{IL}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High–Level Input Voltage	V_{IH}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I_{in}	15	V_{in} = 0 or V_{DD}	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Capacitance	C_{in}	—		—	—	—	5.0	7.5	—	—	pF
SWITCHES IN/OUT AND COMMONS OUT/IN — W, X, Y, Z (Voltages Referenced to V_{EE})											
Recommended Peak–to–Peak Voltage Into or Out of the Switch	$V_{I/O}$	—	Channel On or Off	0	V_{DD}	0	—	V_{DD}	0	V_{DD}	V_{p-p}
Recommended Static or Dynamic Voltage Across the Switch (5.) (Figure 3)	ΔV_{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V_{OO}	—	V_{in} = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R_{on}	5.0 10 15	$\Delta V_{switch} \leq 500$ mV (5.), $V_{in} = V_{IL}$ or V_{IH} (Control), and V_{in} = 0 to V_{DD} (Switch)	— —	800 400 220	— — —	250 120 80	1050 500 280	— — —	1200 520 300	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5.0 10 15		— — —	70 50 45	— — —	25 10 10	70 50 45	— — —	135 95 65	Ω
Off–Channel Leakage Current (Figure 8)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	—	Switch Off	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	$C_{O/I}$	—		—	—	—	17	—	—	—	pF
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	— —	Pins Not Adjacent Pins Adjacent	— —	— —	— —	0.15 0.47	— —	— —	— —	pF

4. Data labeled “Typ” is not to be used for design purposes, but is intended as an indication of the IC’s potential performance.
5. For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS (C_L = 50 pF, T_A = 25°C, $V_{EE} \leq V_{SS}$)

Characteristic	Symbol	$V_{DD} - V_{EE}$ Vdc	Min	Typ (6.)	Max	Unit
Propagation Delay Times Switch Input to Switch Output (R_L = 10 kΩ) t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 26.5 ns t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 11 ns t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 9.0 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 35 15 12	 90 40 30	ns
Control Input to Output (R_L = 10 kΩ) V_{EE} = V_{SS} (Figure 4)	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 350 140 100	 875 350 250	ns
Second Harmonic Distortion R_L = 10 kΩ, f = 1 kHz, V_{in} = 5 V_{p-p}	—	10	—	0.07	—	%
Bandwidth (Figure 5) R_L = 1 kΩ, V_{in} = 1/2 ($V_{DD} - V_{EE}$) $_{p-p}$, 20 Log (V_{out}/V_{in}) = – 3 dB, C_L = 50 pF	BW	10	—	17	—	MHz
Off Channel Feedthrough Attenuation, Figure 5 R_L = 1 kΩ, V_{in} = 1/2 ($V_{DD} - V_{EE}$) $_{p-p}$, f_{in} = 55 MHz	—	10	—	– 50	—	dB
Channel Separation (Figure 6) R_L = 1 kΩ, V_{in} = 1/2 ($V_{DD} - V_{EE}$) $_{p-p}$, f_{in} = 3 MHz	—	10	—	– 50	—	dB
Crosstalk, Control Input to Common O/I, Figure 7 R1 = 1 kΩ, R_L = 10 kΩ, Control t_r = t_f = 20 ns	—	10	—	75	—	mV

6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

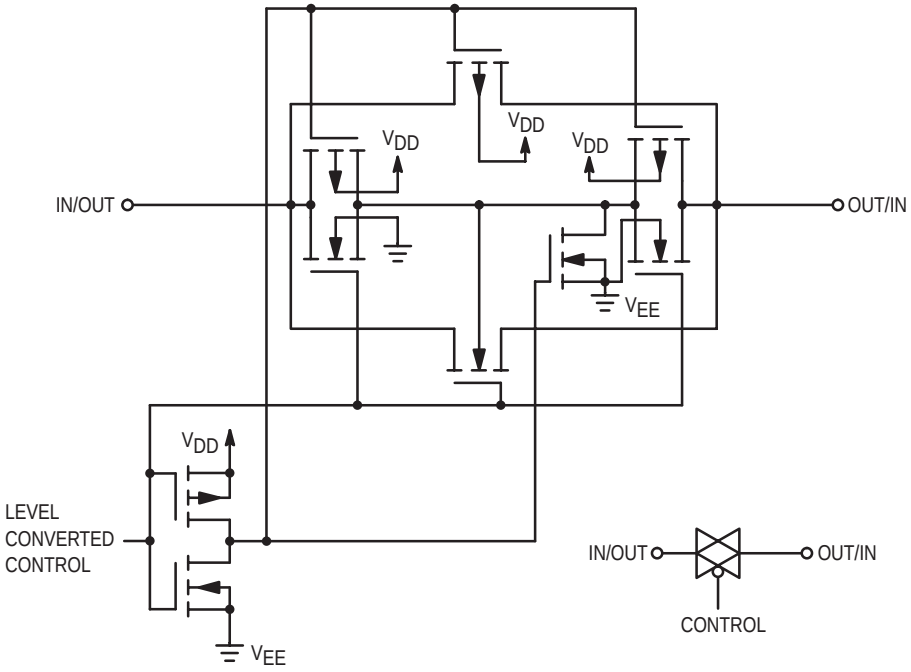


Figure 1. Switch Circuit Schematic

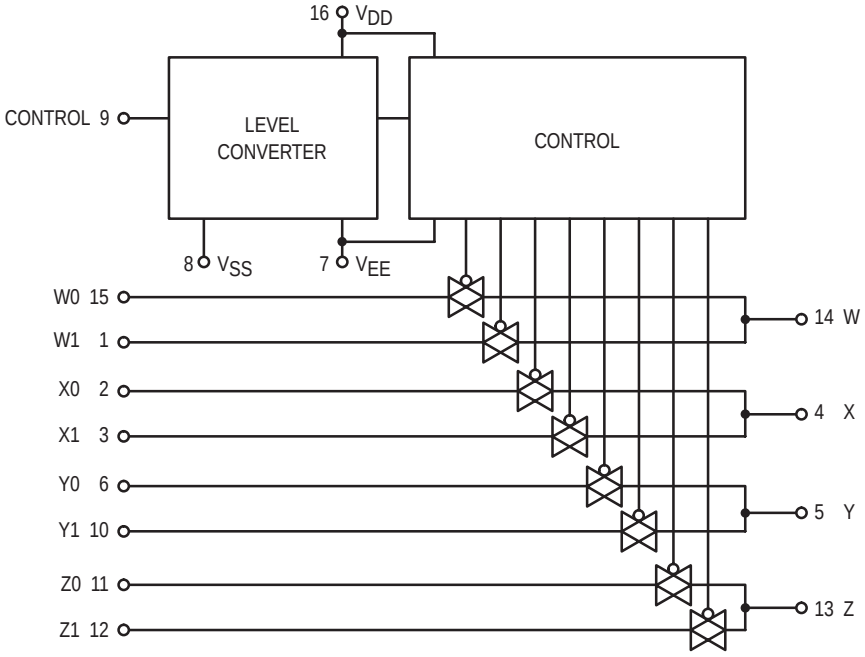


Figure 2. MC14551B Functional Diagram

TEST CIRCUITS

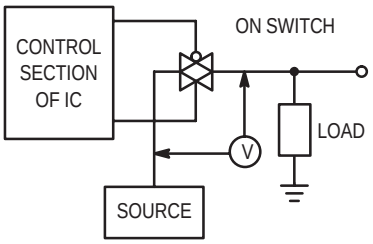


Figure 3. ΔV Across Switch

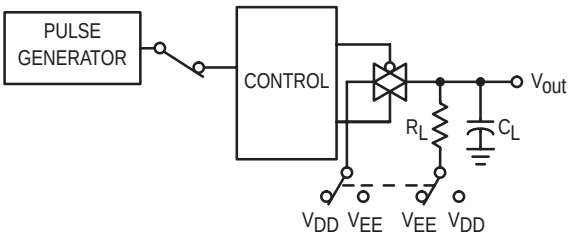


Figure 4. Propagation Delay Times, Control to Output

Control input used to turn ON or OFF the switch under test.

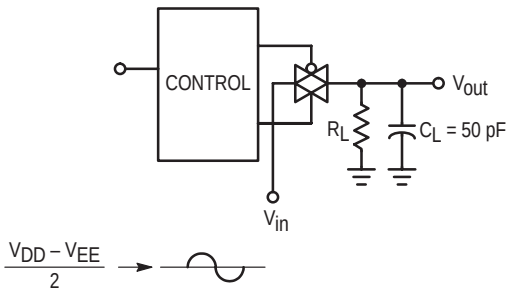


Figure 5. Bandwidth and Off–Channel Feedthrough Attenuation

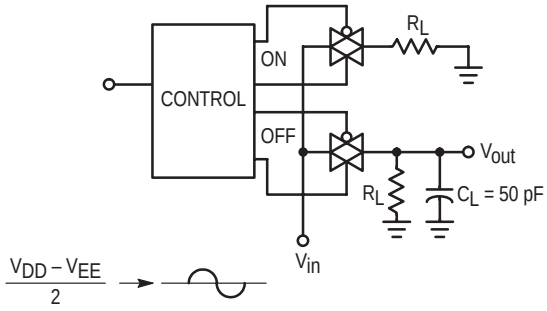


Figure 6. Channel Separation (Adjacent Channels Used for Setup)

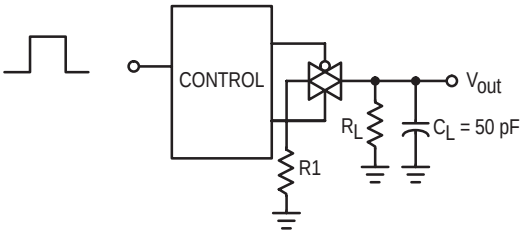


Figure 7. Crosstalk, Control Input to Common O/I

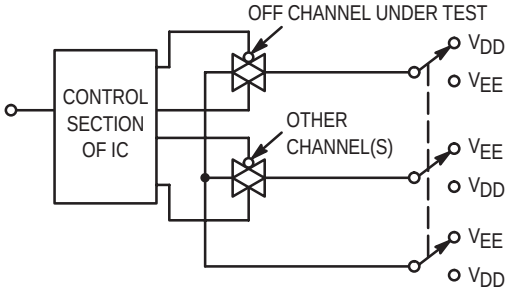


Figure 8. Off Channel Leakage

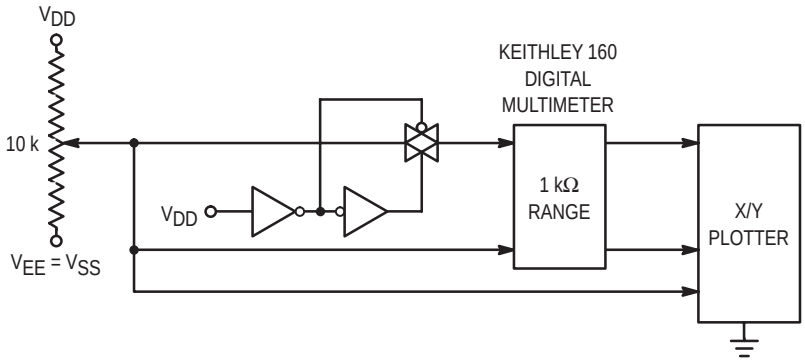


Figure 9. Channel Resistance (R_{ON}) Test Circuit

TYPICAL RESISTANCE CHARACTERISTICS

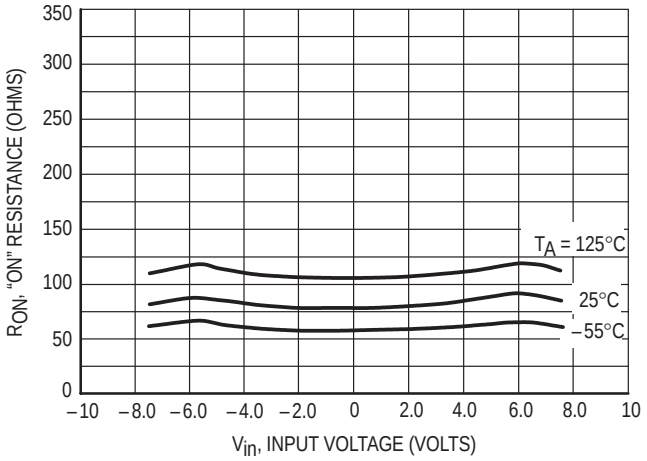


Figure 10. V_{DD} @ 7.5 V, V_{EE} @ – 7.5 V

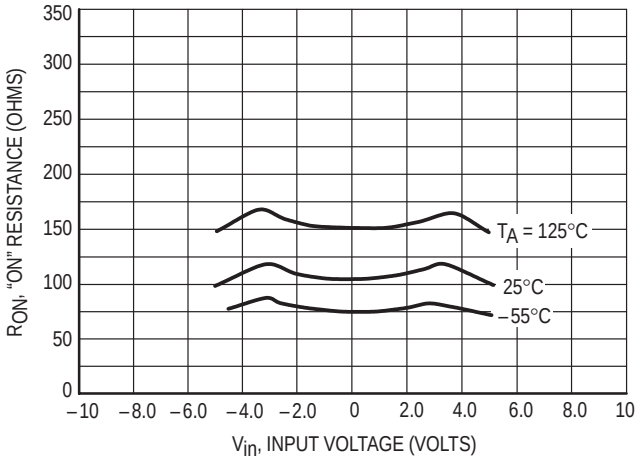


Figure 11. V_{DD} @ 5.0 V, V_{EE} @ – 5.0 V

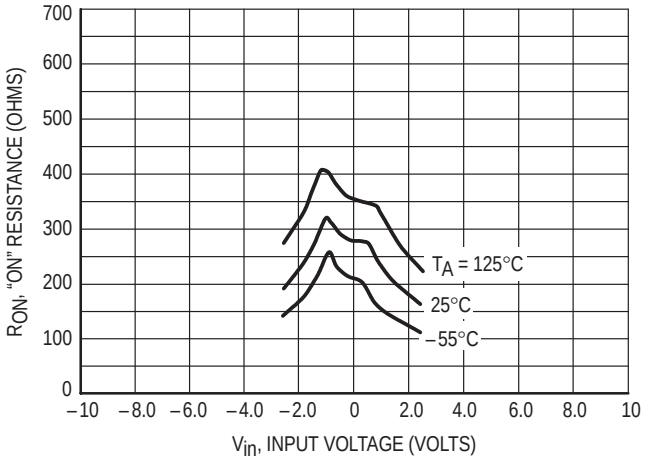


Figure 12. V_{DD} @ 2.5 V, V_{EE} @ – 2.5 V

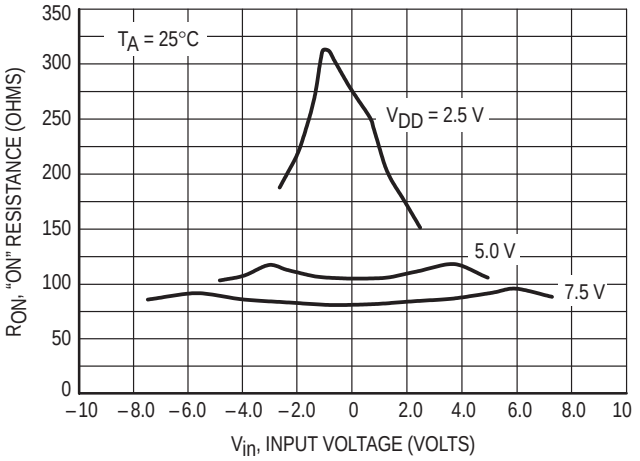


Figure 13. Comparison at 25°C, V_{DD} @ – V_{EE}

APPLICATIONS INFORMATION

Figure A illustrates use of the on–chip level converter detailed in Figure 2. The 0–to–5 volt Digital Control signal is used to directly control a 9 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = + 5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{EE}. The V_{DD} voltage determines the maximum recommended peak above V_{SS}. The V_{EE} voltage determines the maximum swing below V_{SS}. For the example, $V_{DD} - V_{SS}$ = 5 volt maximum swing above V_{SS}; $V_{SS} - V_{EE}$ = 5 volt maximum swing below V_{SS}. The example shows a ± 4.5 volt signal which allows a 1/2 volt margin at each peak. If voltage transients above V_{DD} and/or below V_{EE} are anticipated on the analog channels, external diodes (D_X) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between V_{DD} and V_{EE} is 18.0 volts. Most parameters are specified up to 15 volts which is the recommended maximum difference between V_{DD} and V_{EE}.

Balanced supplies are not required. However, V_{SS} must be greater than or equal to V_{EE}. For example, V_{DD} = + 10 volts, V_{SS} = + 5 volts, and V_{EE} = – 3 volts is acceptable. See the table below.

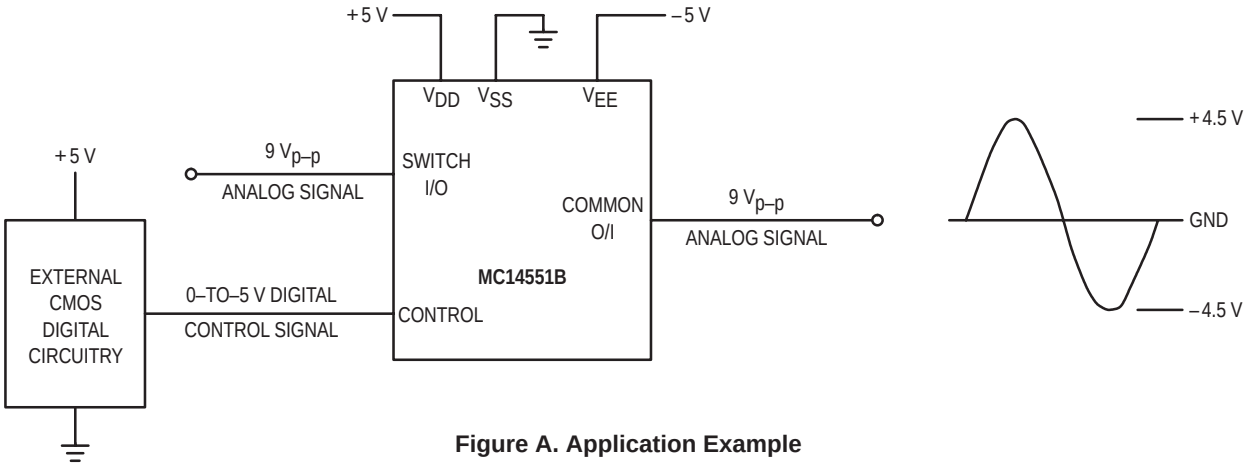


Figure A. Application Example

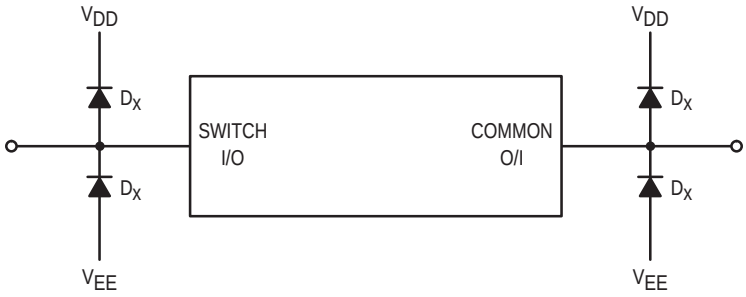


Figure B. External Schottky or Germanium Clipping Diodes

POSSIBLE SUPPLY CONNECTIONS

V_{DD} In Volts	V_{SS} In Volts	V_{EE} In Volts	Control Inputs Logic High/Logic Low In Volts	Maximum Analog Signal Range In Volts
+ 8	0	– 8	+ 8/0	+ 8 to – 8 = 16 V_{p-p}
+ 5	0	– 12	+ 5/0	+ 5 to – 12 = 17 V_{p-p}
+ 5	0	0	+ 5/0	+ 5 to 0 = 5 V_{p-p}
+ 5	0	– 5	+ 5/0	+ 5 to – 5 = 10 V_{p-p}
+ 10		– 5	+ 10/ + 5	+ 10 to – 5 = 15 V_{p-p}

MC74HC4051A, MC74HC4052A, MC74HC4053A

Analog Multiplexers / Demultiplexers

High–Performance Silicon–Gate CMOS

The MC74HC4051A, MC74HC4052A and MC74HC4053A utilize silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The HC4051A, HC4052A and HC4053A are identical in pinout to the metal–gate MC14051AB, MC14052AB and MC14053AB. The Channel–Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel–Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors they are compatible with LSTTL outputs.

These devices have been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal–gate CMOS analog switches.

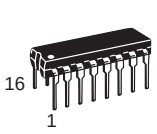
For a multiplexer/demultiplexer with injection current protection, see HC4851A and HC4852A.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ($V_{CC} – V_{EE}$) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range ($V_{CC} – GND$) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal–Gate Counterparts
- Low Noise
- In Compliance With the Requirements of JEDEC Standard No. 7A
- Chip Complexity: HC4051A — 184 FETs or 46 Equivalent Gates
  HC4052A — 168 FETs or 42 Equivalent Gates
  HC4053A — 156 FETs or 39 Equivalent Gates

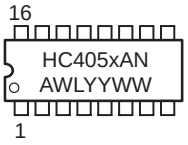
ON Semiconductor

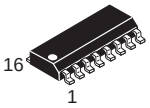
http://onsemi.com

MARKING DIAGRAMS

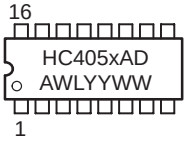


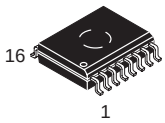
PDIP–16
N SUFFIX
CASE 648



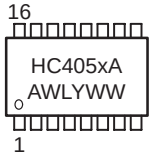


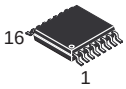
SO–16
D SUFFIX
CASE 751B



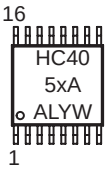


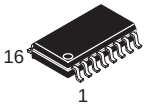
SO–16 WIDE
DW SUFFIX
CASE 751G



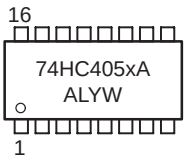


TSSOP–16
DT SUFFIX
CASE 948F





SOEIAJ–16
F SUFFIX
CASE 966

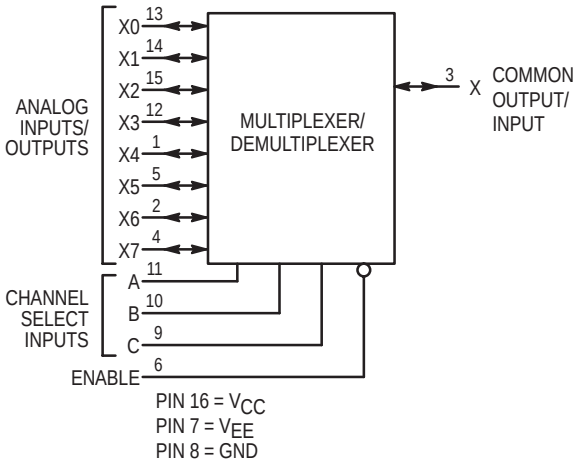


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 67 of this data sheet.

LOGIC DIAGRAM
MC74HC4051A
Single–Pole, 8–Position Plus Common Off

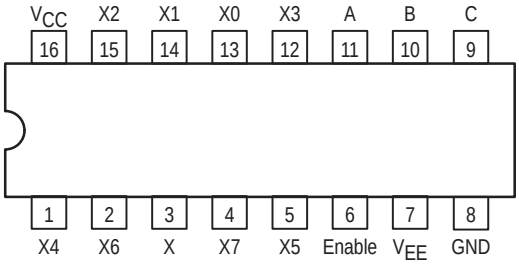


FUNCTION TABLE – MC74HC4051A

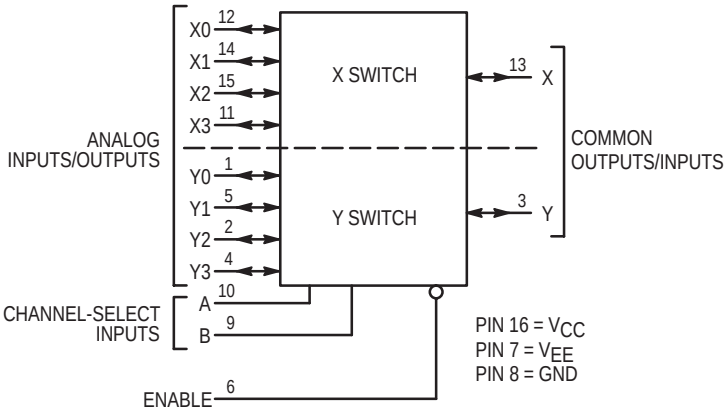
Control Inputs				
	Select			
Enable	C	B	A	ON Channels
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

X = Don't Care

Pinout: MC74HC4051A (Top View)



LOGIC DIAGRAM
MC74HC4052A
Double–Pole, 4–Position Plus Common Off

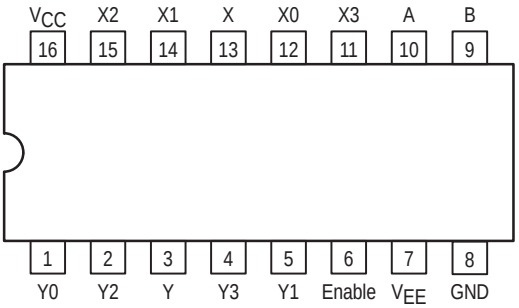


FUNCTION TABLE – MC74HC4052A

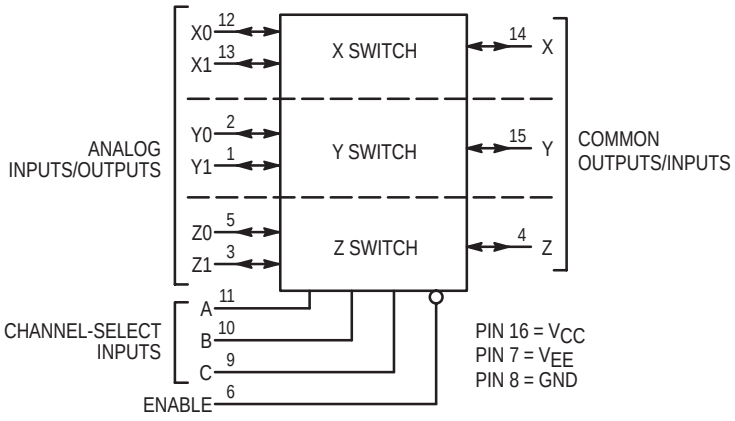
Control Inputs			
	Select		
Enable	B	A	ON Channels
L	L	L	Y0 X0
L	L	H	Y1 X1
L	H	L	Y2 X2
L	H	H	Y3 X3
H	X	X	NONE

X = Don't Care

Pinout: MC74HC4052A (Top View)



LOGIC DIAGRAM
MC74HC4053A
Triple Single–Pole, Double–Position Plus Common Off



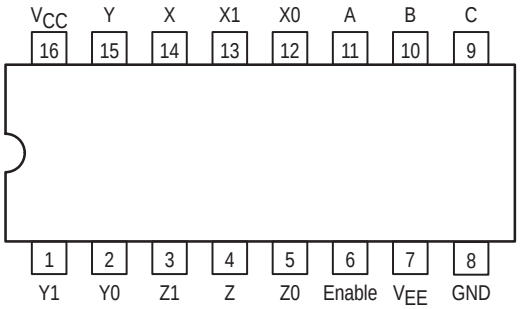
NOTE: This device allows independent control of each switch. Channel–Select Input A controls the X–Switch, Input B controls the Y–Switch and Input C controls the Z–Switch

FUNCTION TABLE – MC74HC4053A

Control Inputs						
	Select			ON Channels		
Enable	C	B	A			
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	NONE		

X = Don't Care

Pinout: MC74HC4053A (Top View)



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	– 0.5 to + 7.0 – 0.5 to + 14.0	V
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	– 7.0 to + 5.0	V
V_{IS}	Analog Input Voltage	V_{EE} – 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin	± 25	mA
P_D	Power Dissipation in Still Air, Plastic DIP† EIAJ/SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
EIAJ/SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	(Referenced to GND) (Referenced to V_{EE})	2.0 2.0	6.0 12.0	V
V_{EE}	Negative DC Supply Voltage, Output (Referenced to GND)		– 6.0	GND	V
V_{IS}	Analog Input Voltage		V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)		GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch			1.2	V
T_A	Operating Temperature Range, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

*For voltage drops across switch greater than 1.2V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) V_{EE} = GND, Except Where Noted

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
I_{in}	Maximum Input Leakage Current, Channel–Select or Enable Inputs	V_{in} = V_{CC} or GND, V_{EE} = – 6.0 V	6.0	± 0.1	± 1.0	± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and V_{IS} = V_{CC} or GND; V_{EE} = GND V_{IO} = 0 V V_{EE} = – 6.0	 6.0 6.0	 1 4	 10 40	 20 80	µA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

DC CHARACTERISTICS — Analog Section

Symbol	Parameter	Condition	V_{CC}	V_{EE}	Guaranteed Limit			Unit
					–55 to 25°C	≤85°C	≤125°C	
R_{on}	Maximum "ON" Resistance	V_{in} = V_{IL} or V_{IH}; V_{IS} = V_{CC} to V_{EE}; $I_S \le 2.0$ mA (Figures 1, 2)	4.5 4.5 6.0	0.0 – 4.5 – 6.0	190 120 100	240 150 125	280 170 140	Ω
		V_{in} = V_{IL} or V_{IH}; V_{IS} = V_{CC} or V_{EE} (Endpoints); $I_S \le 2.0$ mA (Figures 1, 2)	4.5 4.5 6.0	0.0 – 4.5 – 6.0	150 100 80	190 125 100	230 140 115	
ΔR_{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V_{in} = V_{IL} or V_{IH}; V_{IS} = 1/2 (V_{CC} – V_{EE}); $I_S \le 2.0$ mA	4.5 4.5 6.0	0.0 – 4.5 – 6.0	30 12 10	35 15 12	40 18 14	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} – V_{EE}; Switch Off (Figure 3)	6.0	– 6.0	0.1	0.5	1.0	μA
	Maximum Off–Channel Leakage Current, Common Channel HC4051A HC4052A HC4053A	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} – V_{EE}; Switch Off (Figure 4)	6.0 6.0 6.0	– 6.0 – 6.0 – 6.0	0.2 0.1 0.1	2.0 1.0 1.0	4.0 2.0 2.0	
I_{on}	Maximum On–Channel Leakage Current, Channel–to–Channel HC4051A HC4052A HC4053A	V_{in} = V_{IL} or V_{IH}; Switch–to–Switch = V_{CC} – V_{EE}; (Figure 5)	6.0 6.0 6.0	– 6.0 – 6.0 – 6.0	0.2 0.1 0.1	2.0 1.0 1.0	4.0 2.0 2.0	μA

AC CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Channel–Select to Analog Output (Figure 9)	2.0 3.0 4.5 6.0	270 90 59 45	320 110 79 65	350 125 85 75	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0 3.0 4.5 6.0	40 25 12 10	60 30 15 13	70 32 18 15	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 6.0	160 70 48 39	200 95 63 55	220 110 76 63	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 6.0	245 115 49 39	315 145 69 58	345 155 83 67	ns
C_{in}	Maximum Input Capacitance, Channel–Select or Enable Inputs		10	10	10	pF
$C_{I/O}$	Maximum Capacitance — Analog I/O		35	35	35	pF
	(All Switches Off) — Common O/I: HC4051A HC4052A HC4053A		130 80 50	130 80 50	130 80 50	
	Feedthrough		1.0	1.0	1.0	

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D)

Symbol	Parameter		Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0 V	Unit
C_{PD}	Power Dissipation Capacitance (Figure 13)*	HC4051A HC4052A HC4053A	45 80 45	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V_{CC} V	V_{EE} V	Limit* 25°C '51	Limit* 25°C '52	Limit* 25°C '53	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 6)	f_{in} = 1MHz Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{OS}; Increase f_{in} Frequency Until dB Meter Reads –3dB; R_L = 50Ω, C_L = 10pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	80 80 80	95 95 95	120 120 120	MHz
—	Off–Channel Feedthrough Isolation (Figure 7)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600Ω, C_L = 50pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	–50 –50 –50			dB
		f_{in} = 1.0MHz, R_L = 50Ω, C_L = 10pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	–40 –40 –40			
—	Feedthrough Noise. Channel–Select Input to Common I/O (Figure 8)	V_{in} ≤ 1MHz Square Wave (t_r = t_f = 6ns); Adjust R_L at Setup so that I_S = 0A; Enable = GND R_L = 600Ω, C_L = 50pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	25 105 135			mV_{PP}
		R_L = 10kΩ, C_L = 10pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	35 145 190			
—	Crosstalk Between Any Two Switches (Figure 12) (Test does not apply to HC4051A)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600Ω, C_L = 50pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	–50 –50 –50			dB
		f_{in} = 1.0MHz, R_L = 50Ω, C_L = 10pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	–60 –60 –60			
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1kHz, R_L = 10kΩ, C_L = 50pF $THD = THD_{measured} - THD_{source}$ V_{IS} = 4.0V_{PP} sine wave V_{IS} = 8.0V_{PP} sine wave V_{IS} = 11.0V_{PP} sine wave	2.25 4.50 6.00	–2.25 –4.50 –6.00	0.10 0.08 0.05			%

*Limits not tested. Determined by design and verified by qualification.

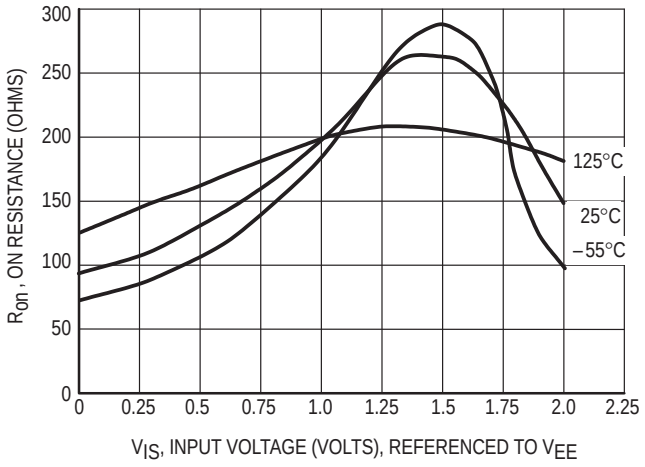


Figure 1a. Typical On Resistance, $V_{CC} - V_{EE}$ = 2.0 V

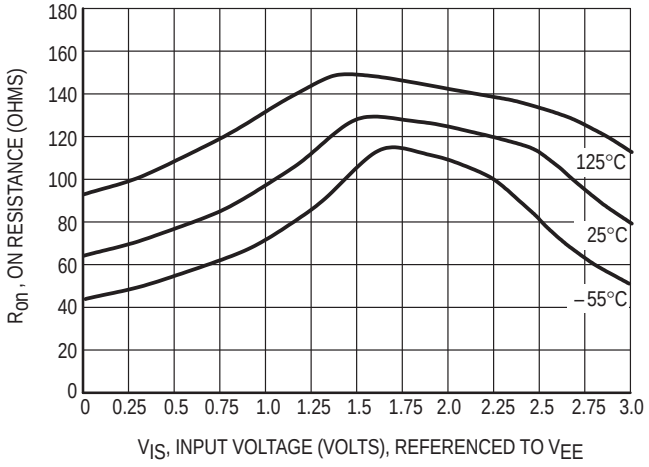


Figure 1b. Typical On Resistance, $V_{CC} - V_{EE}$ = 3.0 V

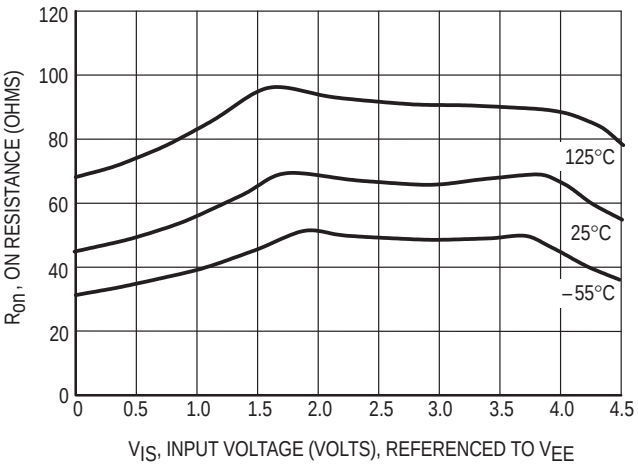


Figure 1c. Typical On Resistance, $V_{CC} - V_{EE}$ = 4.5 V

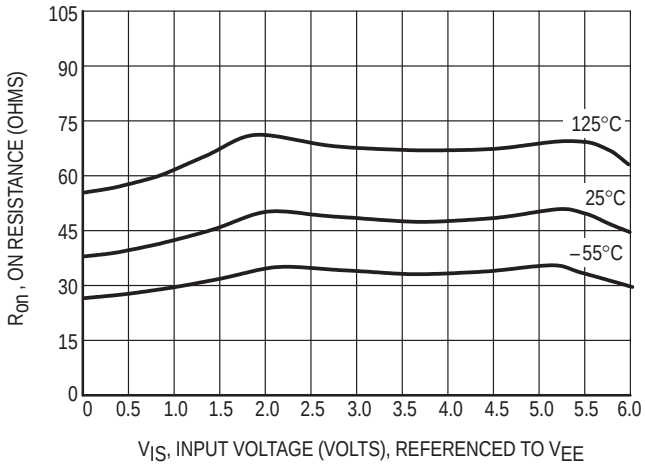


Figure 1d. Typical On Resistance, $V_{CC} - V_{EE}$ = 6.0 V

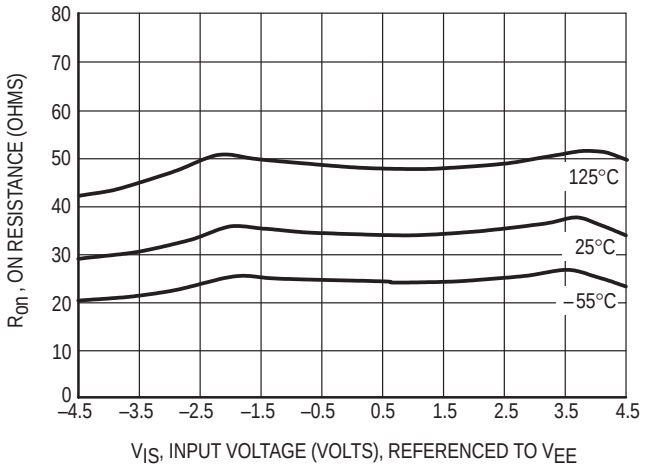


Figure 1e. Typical On Resistance, $V_{CC} - V_{EE}$ = 9.0 V

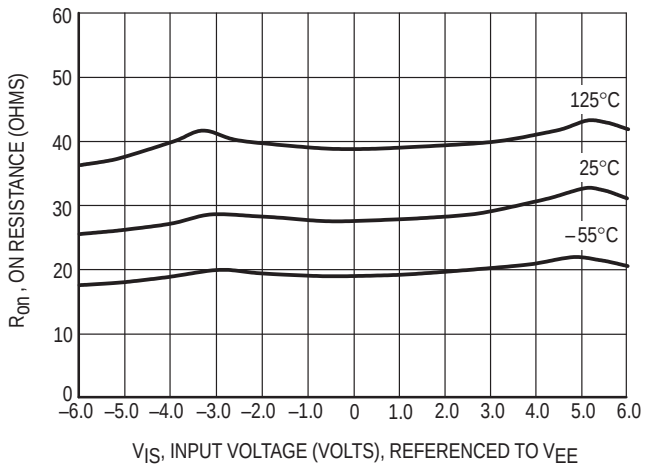


Figure 1f. Typical On Resistance, $V_{CC} - V_{EE}$ = 12.0 V

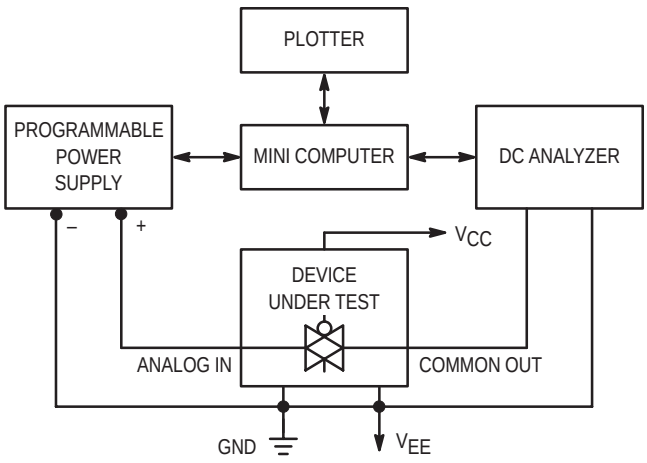


Figure 2. On Resistance Test Set–Up

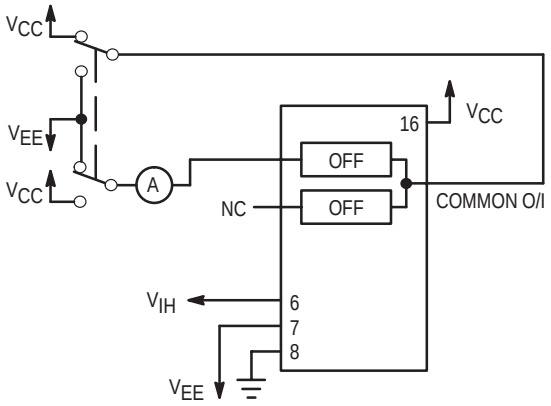


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

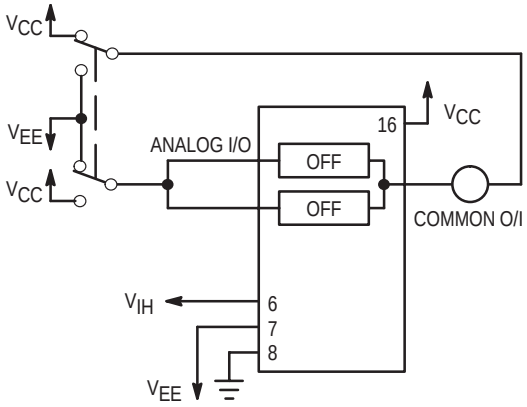


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set–Up

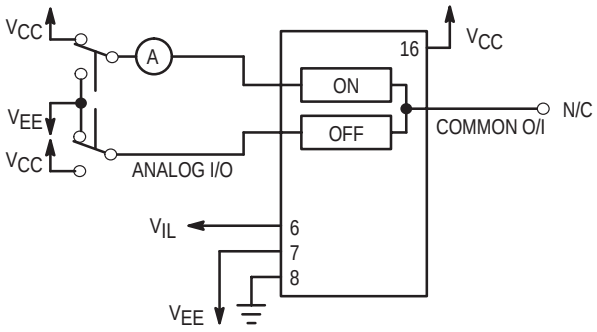


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set–Up

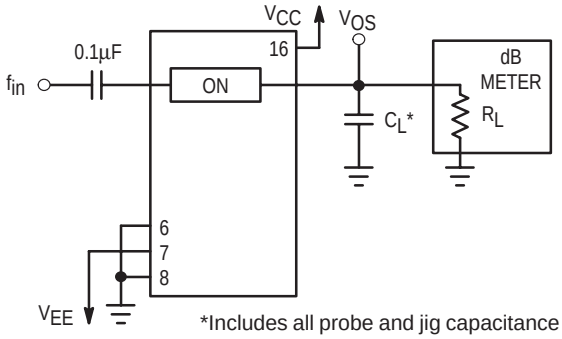


Figure 6. Maximum On Channel Bandwidth, Test Set–Up

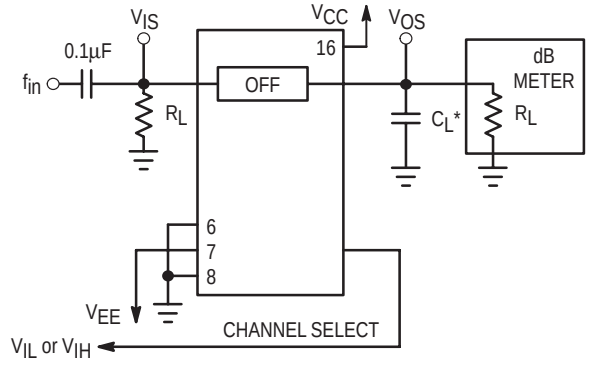


Figure 7. Off Channel Feedthrough Isolation, Test Set–Up

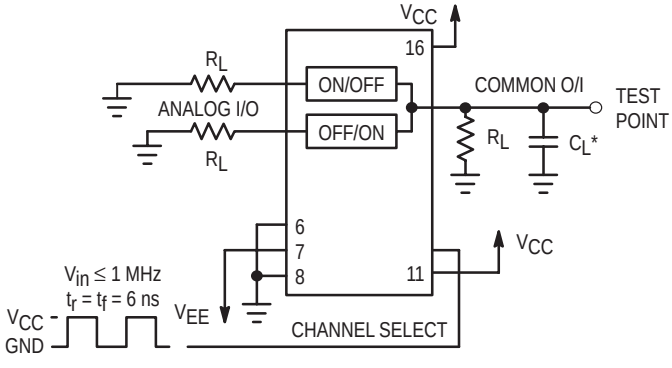


Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set–Up

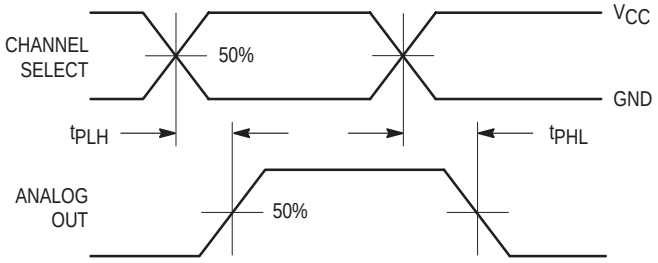
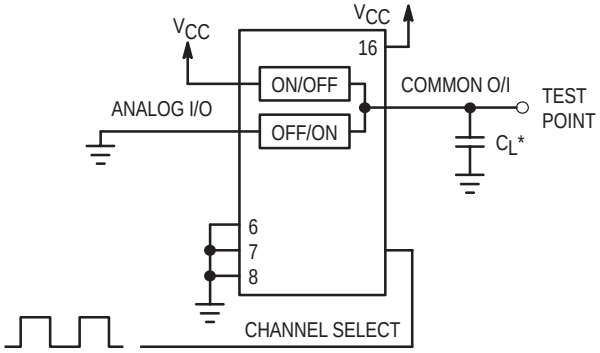


Figure 9a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 9b. Propagation Delay, Test Set–Up Channel Select to Analog Out

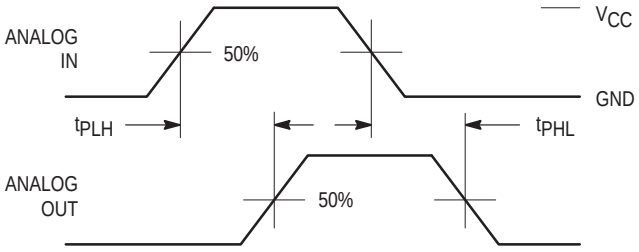
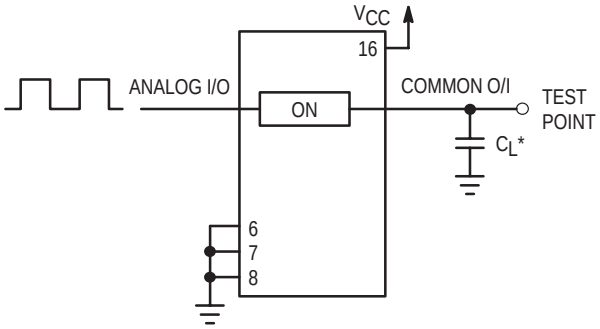


Figure 10a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 10b. Propagation Delay, Test Set–Up Analog In to Analog Out

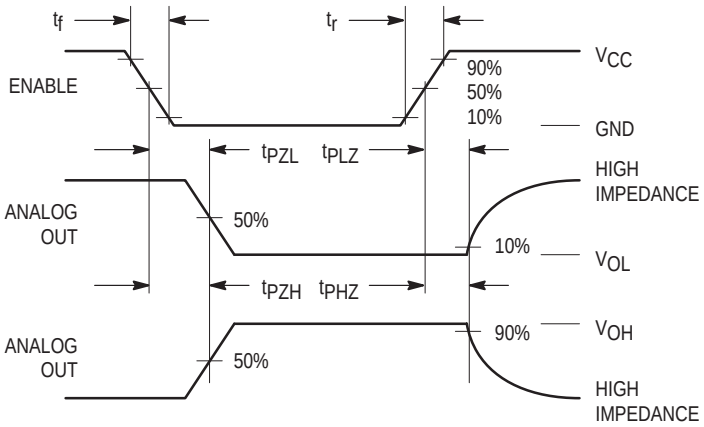


Figure 11a. Propagation Delays, Enable to Analog Out

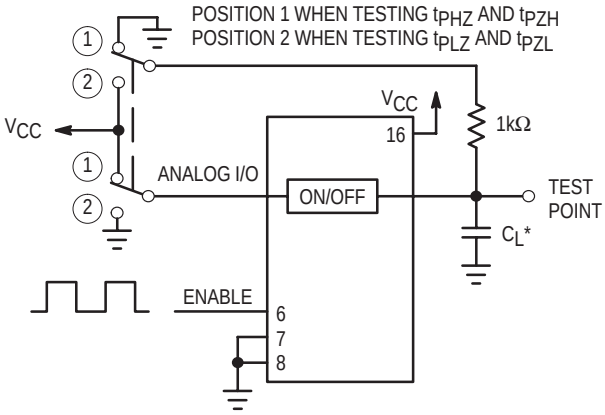


Figure 11b. Propagation Delay, Test Set–Up Enable to Analog Out

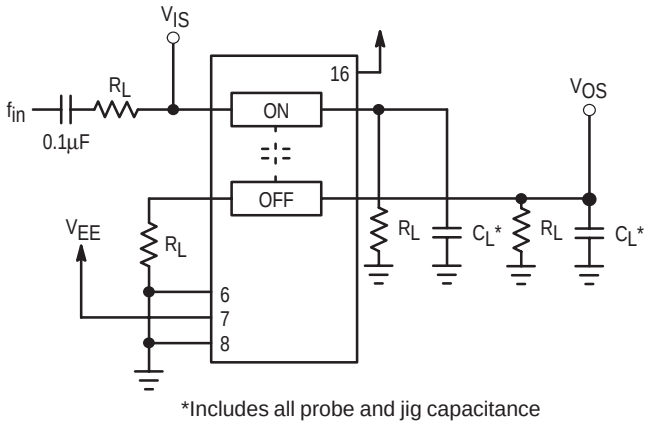


Figure 12. Crosstalk Between Any Two Switches, Test Set–Up

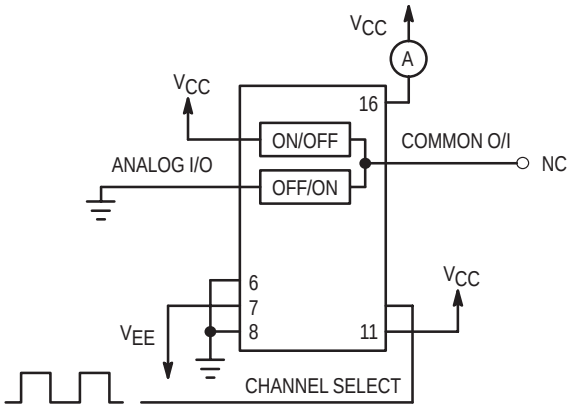


Figure 13. Power Dissipation Capacitance, Test Set–Up

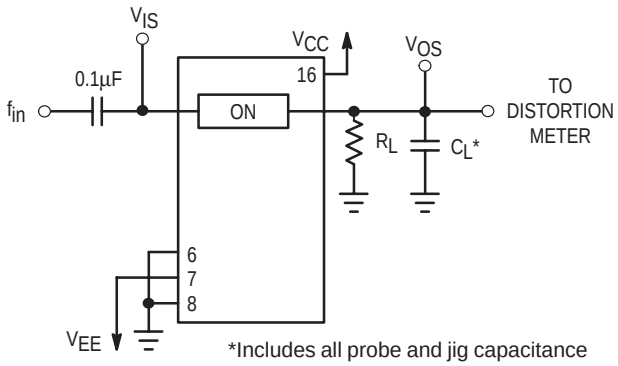


Figure 14a. Total Harmonic Distortion, Test Set–Up

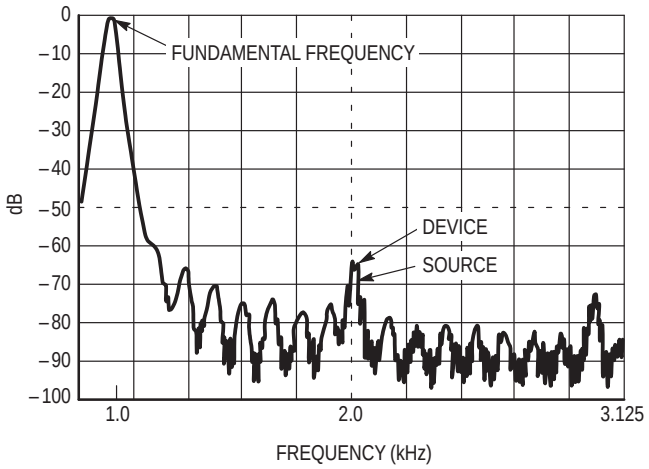


Figure 14b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

V_{CC} = +5V = logic high
GND = 0V = logic low

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below V_{EE}. In this example, the difference between V_{CC} and V_{EE} is ten volts. Therefore, using the configuration of Figure 15, a maximum analog signal of ten volts peak–to–peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

V_{CC} – GND = 2 to 6 volts
V_{EE} – GND = 0 to –6 volts
V_{CC} – V_{EE} = 2 to 12 volts
and $V_{EE} \leq$ GND

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external Germanium or Schottky diodes (D_X) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

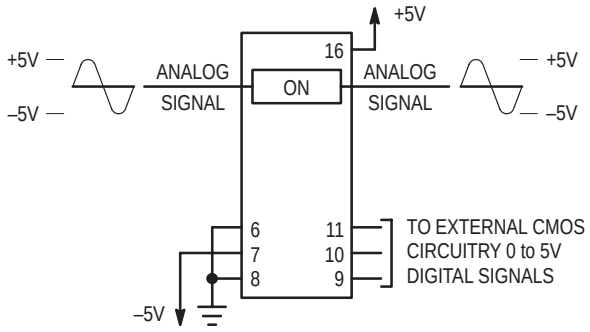


Figure 15. Application Example

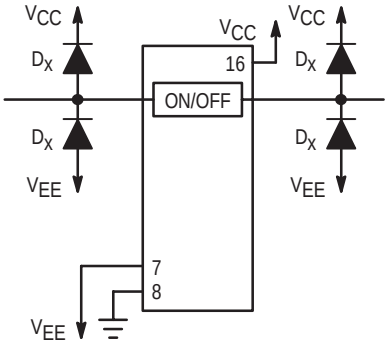
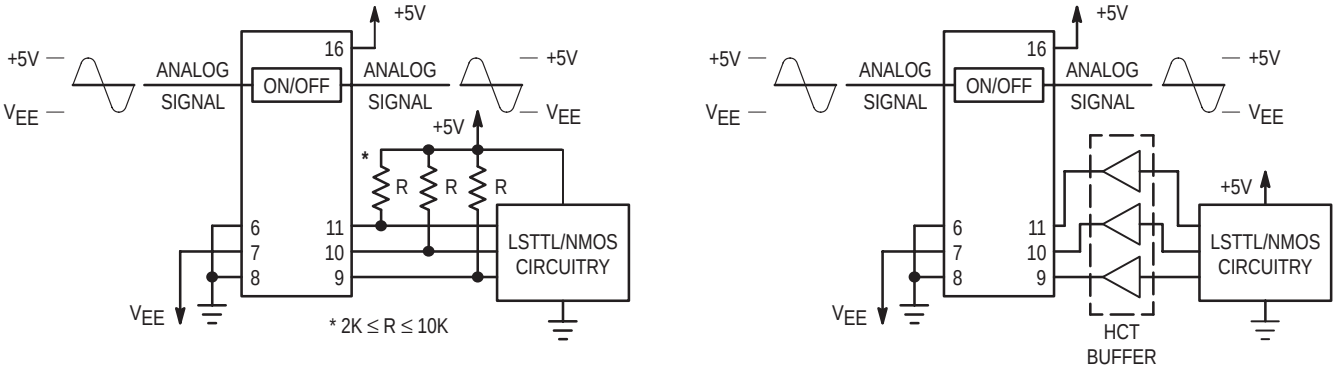


Figure 16. External Germanium or Schottky Clipping Diodes



a. Using Pull–Up Resistors

b. Using HCT Interface

Figure 17. Interfacing LSTTL/NMOS to CMOS Inputs

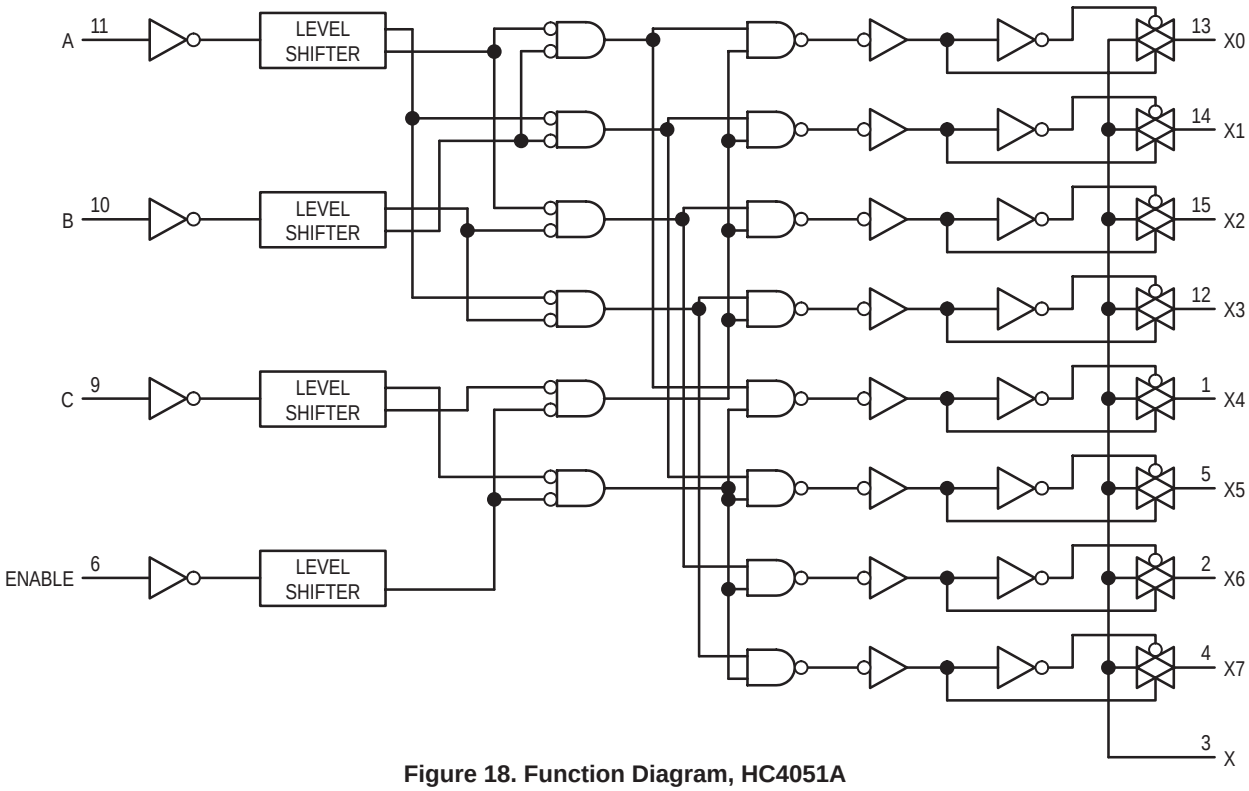


Figure 18. Function Diagram, HC4051A

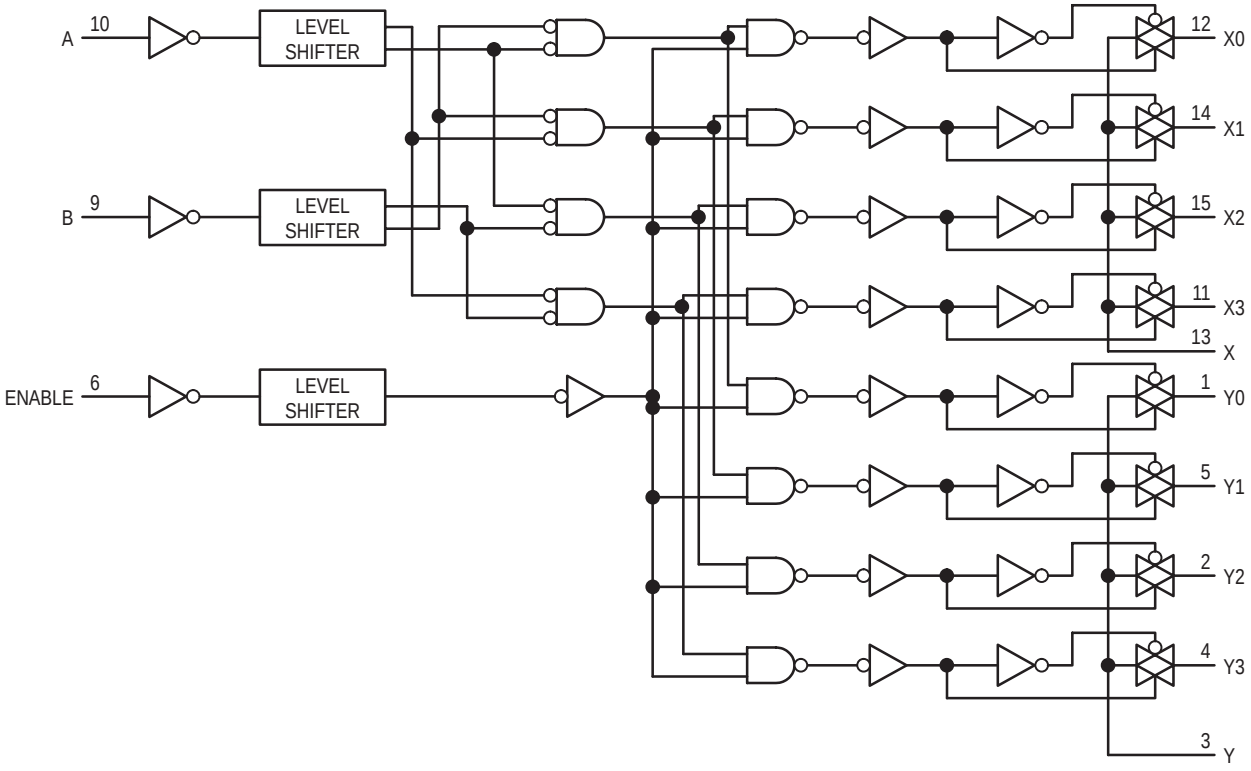


Figure 19. Function Diagram, HC4052A

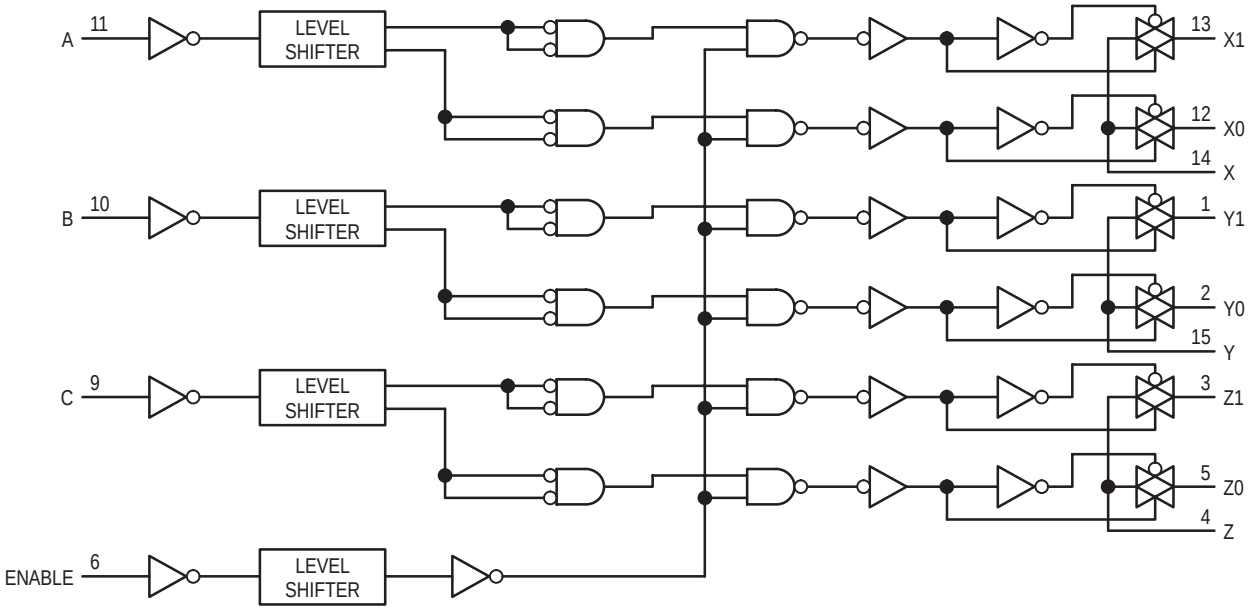


Figure 20. Function Diagram, HC4053A

ORDERING & SHIPPING INFORMATION

Device	Package	Shipping
MC74HC4051AN	PDIP–16	500 Units / Unit Pak
MC74HC4051AD	SOIC–16	48 Units / Rail
MC74HC4051ADR2	SOIC–16	2500 Units / Tape & Reel
MC74HC4051ADT	TSSOP–16	96 Units / Rail
MC74HC4051ADTR2	TSSOP–16	2500 Units / Tape & Reel
MC74HC4051ADW	SOIC WIDE	48 Units / Rail
MC74HC4051ADWR2	SOIC WIDE	1000 Units / Tape & Reel
MC74HC4051AF	SOEIAJ–16	See Note 1.
MC74HC4051AFEL	SOEIAJ–16	See Note 1.
MC74HC4052AN	PDIP–16	500 Units / Unit Pak
MC74HC4052AD	SOIC–16	48 Units / Rail
MC74HC4052ADR2	SOIC–16	2500 Units / Tape & Reel
MC74HC4052ADT	TSSOP–16	96 Units / Rail
MC74HC4052ADTR2	TSSOP–16	2500 Units / Tape & Reel
MC74HC4052ADW	SOIC WIDE	48 Units / Rail
MC74HC4052ADWR2	SOIC WIDE	1000 Units / Tape & Reel
MC74HC4052AF	SOEIAJ–16	See Note 1.
MC74HC4052AFEL	SOEIAJ–16	See Note 1.
MC74HC4053AN	PDIP–16	500 Units / Unit Pak
MC74HC4053AD	SOIC–16	48 Units / Rail
MC74HC4053ADR2	SOIC–16	2500 Units / Tape & Reel
MC74HC4053ADT	TSSOP–16	96 Units / Rail
MC74HC4053ADTR2	TSSOP–16	2500 Units / Tape & Reel
MC74HC4053ADW	SOIC WIDE	48 Units / Rail
MC74HC4053ADWR2	SOIC WIDE	1000 Units / Tape & Reel
MC74HC4053AF	SOEIAJ–16	See Note 1.
MC74HC4053AFEL	SOEIAJ–16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

MC74HC4066A

Advance Information

Quad Analog Switch/ Multiplexer/Demultiplexer

High–Performance Silicon–Gate CMOS

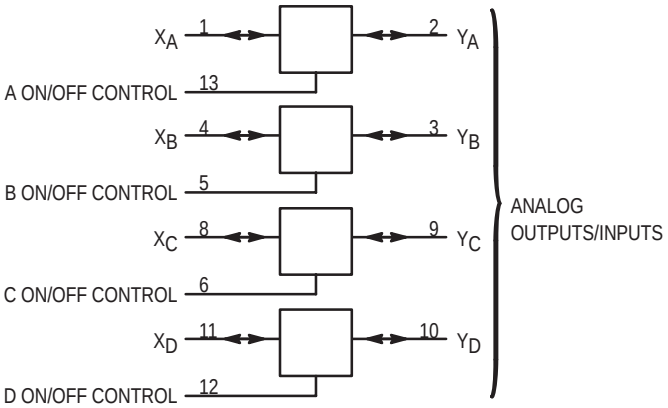
The MC74HC4066A utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF–channel leakage current. This bilateral switch/ multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power–supply range (from V_{CC} to GND).

The HC4066A is identical in pinout to the metal–gate CMOS MC14016 and MC14066. Each device has four independent switches. The device has been designed so that the ON resistances (R_{ON}) are much more linear over input voltage than R_{ON} of metal–gate CMOS analog switches.

The ON/OFF control inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. For analog switches with voltage–level translators, see the HC4316A.

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power–Supply Voltage Range (V_{CC} – GND) = 2.0 to 12.0 Volts
- Analog Input Voltage Range (V_{CC} – GND) = 2.0 to 12.0 Volts
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14016 or MC14066
- Low Noise
- Chip Complexity: 44 FETs or 11 Equivalent Gates

LOGIC DIAGRAM



ANALOG INPUTS/OUTPUTS = X_A, X_B, X_C, X_D
PIN 14 = V_{CC}
PIN 7 = GND

FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ON Semiconductor

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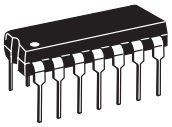
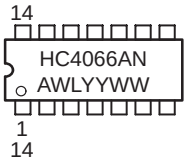
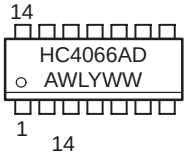
MARKING DIAGRAMS

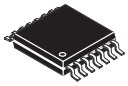


PDIP–14
N SUFFIX
CASE 646

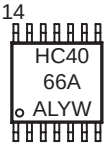


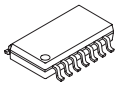
SOIC–14
D SUFFIX
CASE 751A



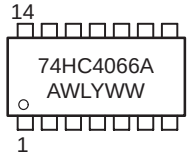


TSSOP–14
DT SUFFIX
CASE 948G



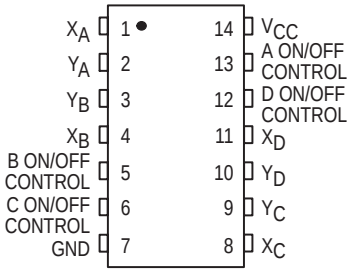


SOEIAJ–14
F SUFFIX
CASE 965



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC4066AN	PDIP–14	2000 / Box
MC74HC4066AD	SOIC–14	55 / Rail
MC74HC4066ADR2	SOIC–14	2500 / Reel
MC74HC4066ADT	TSSOP–14	96 / Rail
MC74HC4066ADTR2	TSSOP–14	2500 / Reel
MC74HC4066AF	SOEIAJ–14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	– 0.5 to + 14.0	V
V_{IS}	Analog Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current Into or Out of Any Pin	± 25	mA
P_D	Power Dissipation in Still Air, Plastic DIP† EIAJ/SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
EIAJ/SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	2.0	12.0	V
V_{IS}	Analog Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch	—	1.2	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time, ON/OFF Control Inputs (Figure 10)			ns
	V_{CC} = 2.0 V	0	1000	
	V_{CC} = 3.0 V	0	600	
	V_{CC} = 4.5 V	0	500	
	V_{CC} = 9.0 V	0	400	
	V_{CC} = 12.0 V	0	250	

*For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTIC Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25°C	Guaranteed Limit ≤ 85°C	Guaranteed Limit ≤ 125°C	Unit
V_{IH}	Minimum High–Level Voltage ON/OFF Control Inputs	R_{on} = Per Spec	2.0 3.0 4.5 9.0 12.0	1.5 2.1 3.15 6.3 8.4	1.5 2.1 3.15 6.3 8.4	1.5 2.1 3.15 6.3 8.4	V
V_{IL}	Maximum Low–Level Voltage ON/OFF Control Inputs	R_{on} = Per Spec	2.0 3.0 4.5 9.0 12.0	0.5 0.9 1.35 2.7 3.6	0.5 0.9 1.35 2.7 3.6	0.5 0.9 1.35 2.7 3.6	V
I_{in}	Maximum Input Leakage Current ON/OFF Control Inputs	V_{in} = V_{CC} or GND	12.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND V_{IO} = 0 V	6.0 12.0	2 4	20 40	40 160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
R_{on}	Maximum "ON" Resistance	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ to GND $I_S \leq 2.0$ mA (Figures 1, 2)	2.0† 3.0† 4.5 9.0 12.0	— — 120 70 70	— — 160 85 85	— — 200 100 100	Ω
		$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or GND (Endpoints) $I_S \leq 2.0$ mA (Figures 1, 2)	2.0 3.0 4.5 9.0 12.0	— — 70 50 30	— — 85 60 60	— — 100 80 80	
ΔR_{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IH}$ V_{IS} = 1/2 (V_{CC} – GND) $I_S \leq 2.0$ mA	2.0 4.5 9.0 12.0	— 20 15 15	— 25 20 20	— 30 25 25	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ $V_{IO} = V_{CC}$ or GND Switch Off (Figure 3)	12.0	0.1	0.5	1.0	μA
I_{on}	Maximum On–Channel Leakage Current, Any One Channel	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or GND (Figure 4)	12.0	0.1	0.5	1.0	μA

†At supply voltage (V_{CC}) approaching 3 V the analog switch–on resistance becomes extremely non–linear. Therefore, for low–voltage operation, it is recommended that these devices only be used to control digital signals.

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, ON/OFF Control Inputs: $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0 3.0 4.5 9.0 12.0	40 30 5 5 5	50 40 7 7 7	60 50 8 8 8	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0 3.0 4.5 9.0 12.0	80 60 20 20 20	90 70 25 25 25	110 80 35 35 35	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 1 1)	2.0 3.0 4.5 9.0 12.0	80 45 20 20 20	90 50 25 25 25	100 60 30 30 30	ns
C	Maximum Capacitance — ON/OFF Control Input	—	10	10	10	pF
	Control Input = GND Analog I/O Feedthrough	— —	35 1.0	35 1.0	35 1.0	

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Switch) (Figure 13)*	15	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Test Conditions	V_{CC} V	Limit* 25°C 54/74HC	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 5)	f_{in} = 1 MHz Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{OS} Increase f_{in} Frequency Until dB Meter Reads – 3 dB R_L = 50 Ω, C_L = 10 pF	4.5 9.0 12.0	150 160 160	MHz
—	Off–Channel Feedthrough Isolation (Figure 6)	f_{in} ≡ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	4.5 9.0 12.0	– 50 – 50 – 50	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	4.5 9.0 12.0	– 40 – 40 – 40	
—	Feedthrough Noise, Control to Switch (Figure 7)	V_{in} ≤ 1 MHz Square Wave (t_r = t_f = 6 ns) Adjust R_L at Setup so that I_S = 0 A R_L = 600 Ω, C_L = 50 pF	4.5 9.0 12.0	60 130 200	mV_{PP}
		R_L = 10 kΩ, C_L = 10 pF	4.5 9.0 12.0	30 65 100	
—	Crosstalk Between Any Two Switches (Figure 12)	f_{in} ≡ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	4.5 9.0 12.0	– 70 – 70 – 70	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	4.5 9.0 12.0	– 80 – 80 – 80	
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1 kHz, R_L = 10 kΩ, C_L = 50 pF $THD = THD_{Measured} - THD_{Source}$ V_{IS} = 4.0 V_{PP} sine wave V_{IS} = 8.0 V_{PP} sine wave V_{IS} = 11.0 V_{PP} sine wave	 4.5 9.0 12.0	 0.10 0.06 0.04	%

*Guaranteed limits not tested. Determined by design and verified by qualification.

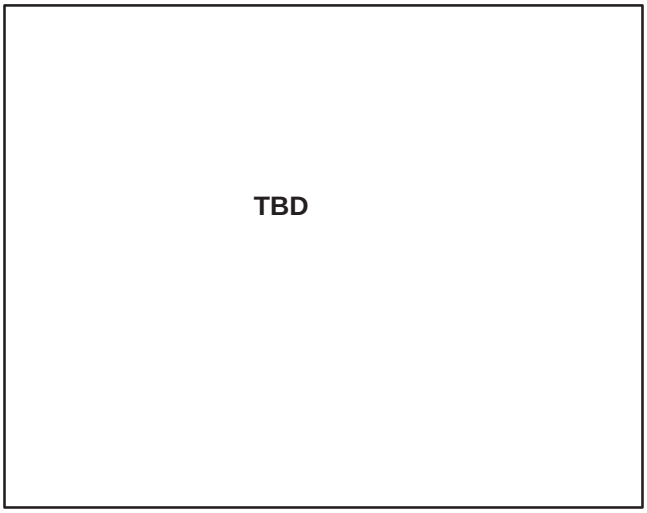


Figure 1a. Typical On Resistance, V_{CC} = 2.0 V

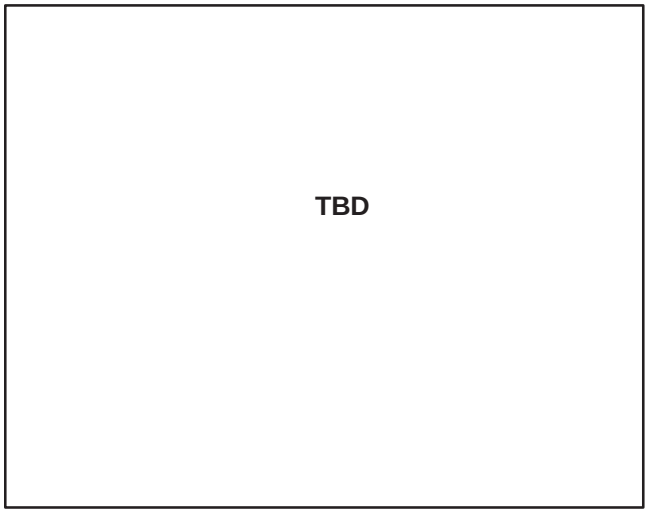


Figure 1b. Typical On Resistance, V_{CC} = 4.5 V

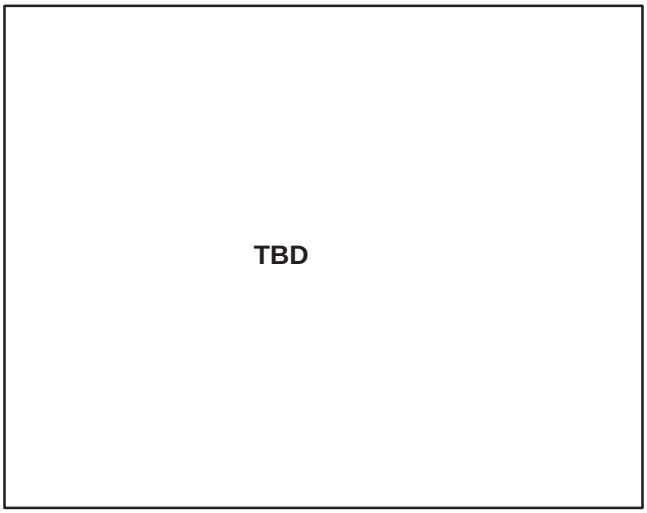


Figure 1c. Typical On Resistance, V_{CC} = 6.0 V

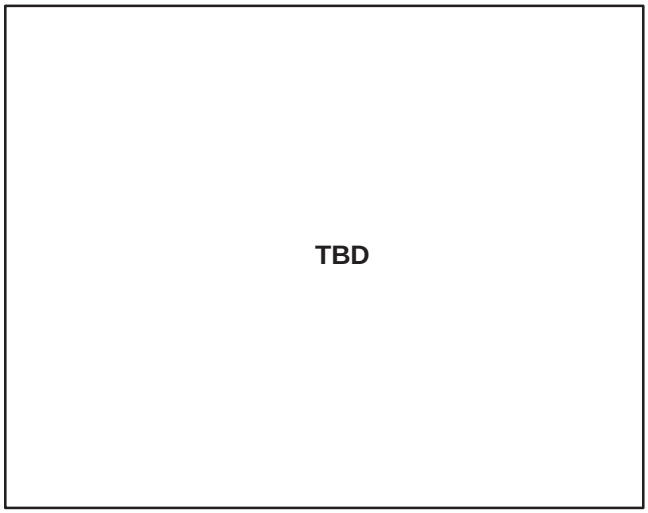


Figure 1d. Typical On Resistance, V_{CC} = 9.0 V

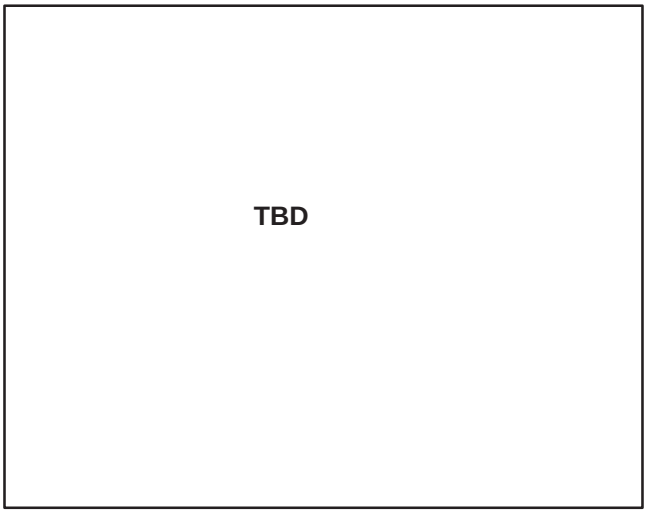


Figure 1e. Typical On Resistance, V_{CC} = 12 V

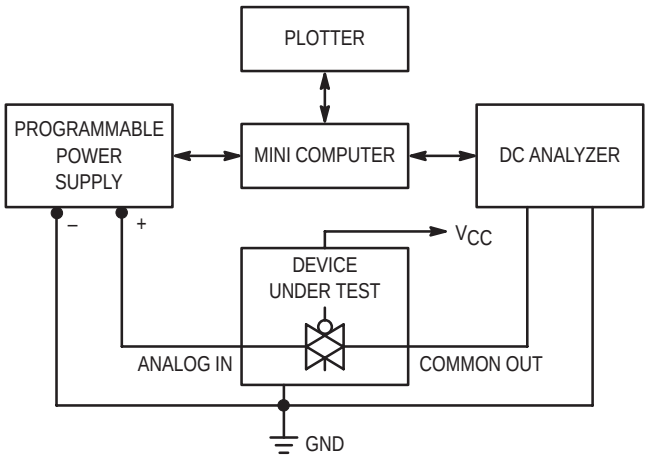


Figure 2. On Resistance Test Set–Up

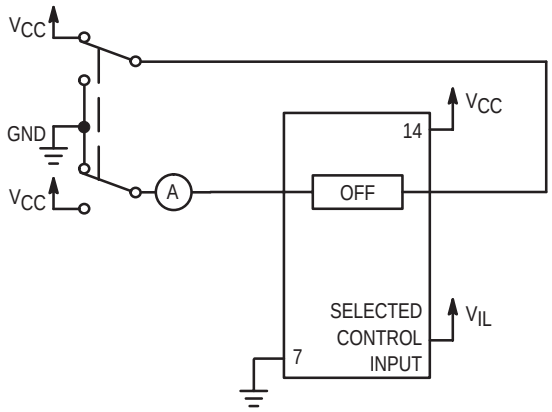


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

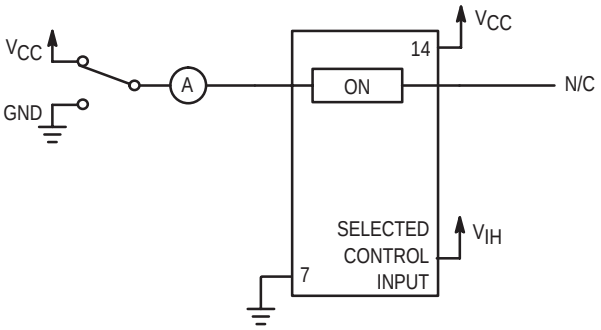
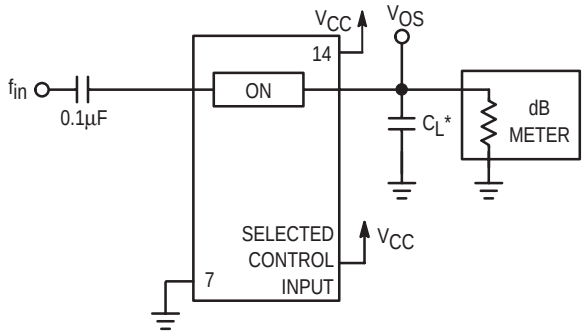
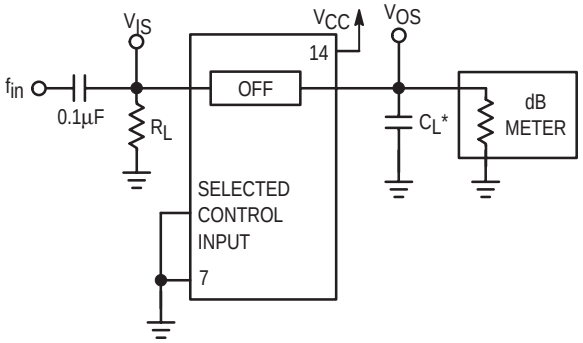


Figure 4. Maximum On Channel Leakage Current, Test Set–Up



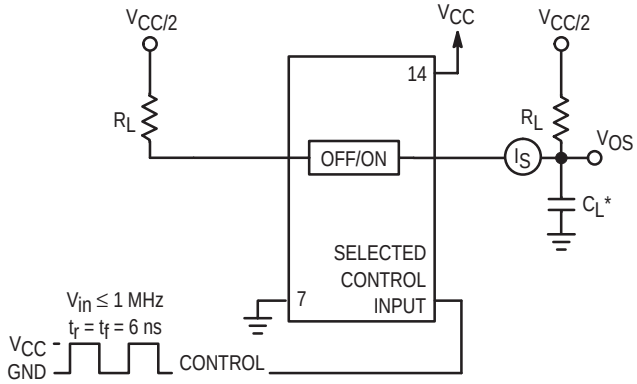
*Includes all probe and jig capacitance.

Figure 5. Maximum On–Channel Bandwidth Test Set–Up



*Includes all probe and jig capacitance.

Figure 6. Off–Channel Feedthrough Isolation, Test Set–Up



*Includes all probe and jig capacitance.

Figure 7. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set–Up

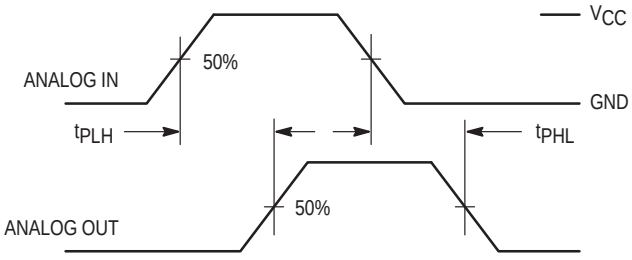
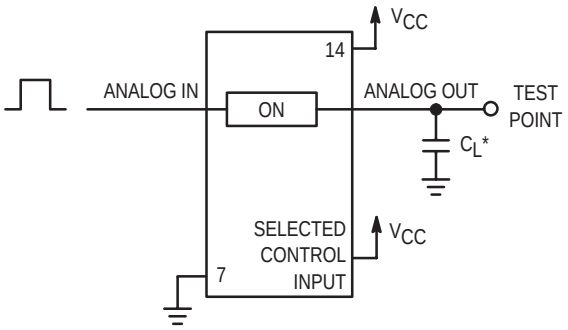


Figure 8. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set–Up

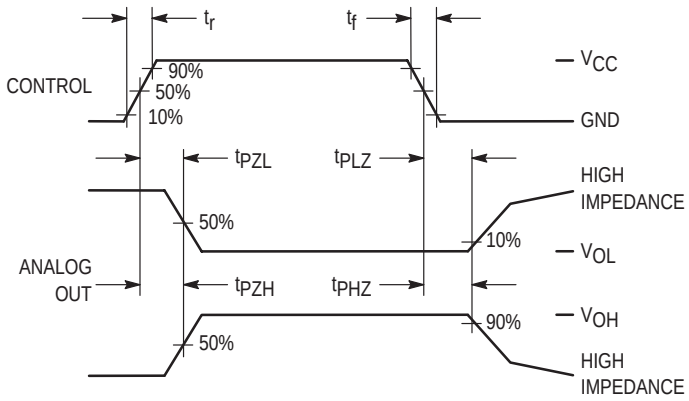
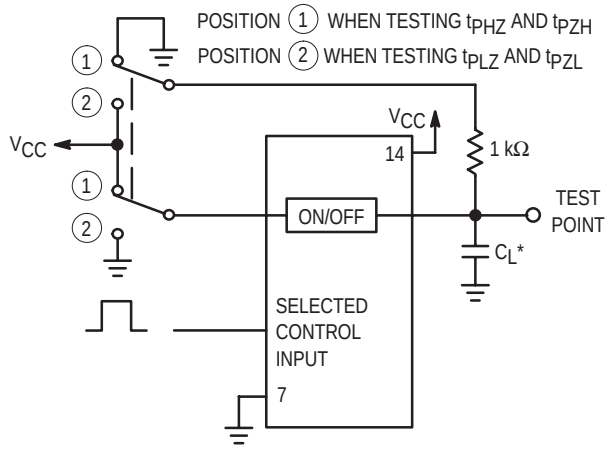
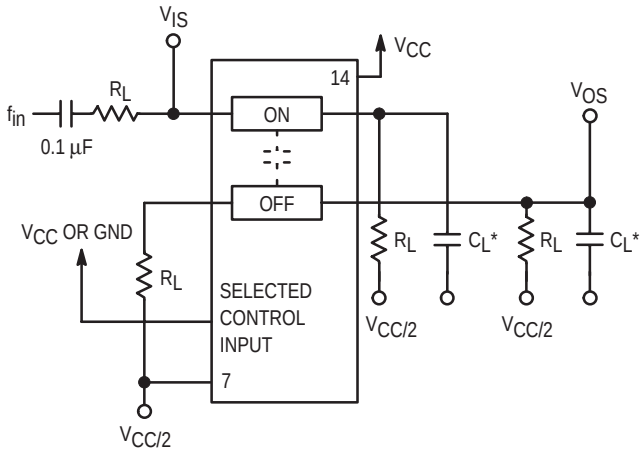


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set–Up



*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set–Up

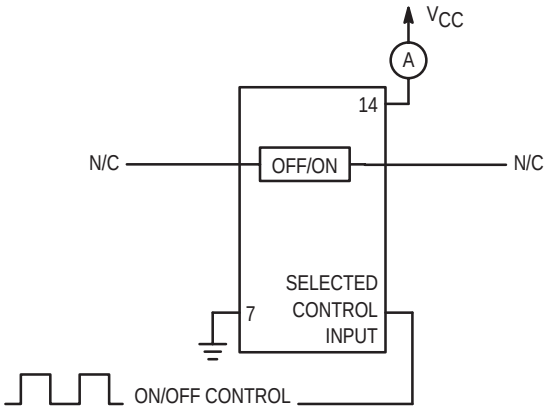
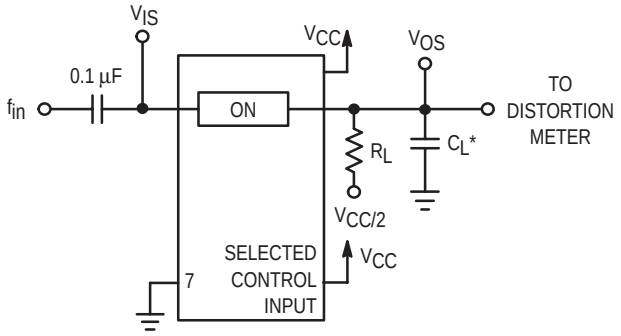


Figure 13. Power Dissipation Capacitance Test Set–Up



*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set–Up

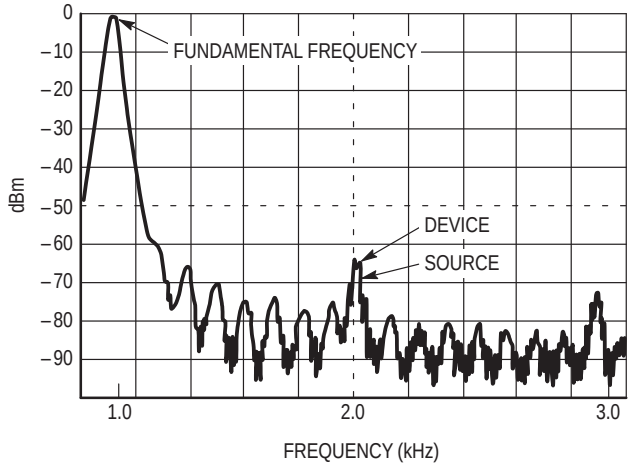


Figure 15. Plot, Harmonic Distortion

APPLICATION INFORMATION

The ON/OFF Control pins should be at V_{CC} or GND logic levels, V_{CC} being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to V_{CC} or GND through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked–up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages V_{CC} and GND. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below GND. In the example below, the difference between V_{CC} and GND is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak–to–peak can be controlled.

When voltage transients above V_{CC} and/or below GND are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure 17. These diodes should be small signal, fast turn–on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the Dx diodes with Mosorbs (Mosorb™ is an acronym for high current surge protectors). Mosorbs are fast turn–on devices ideally suited for precise DC protection with no inherent wear out mechanism.

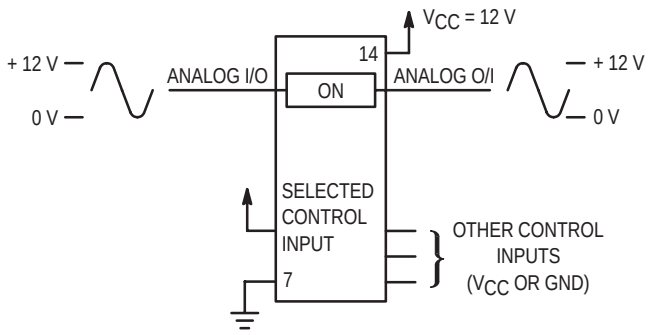


Figure 16. 12 V Application

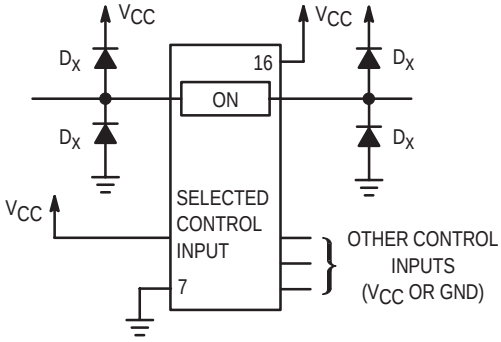
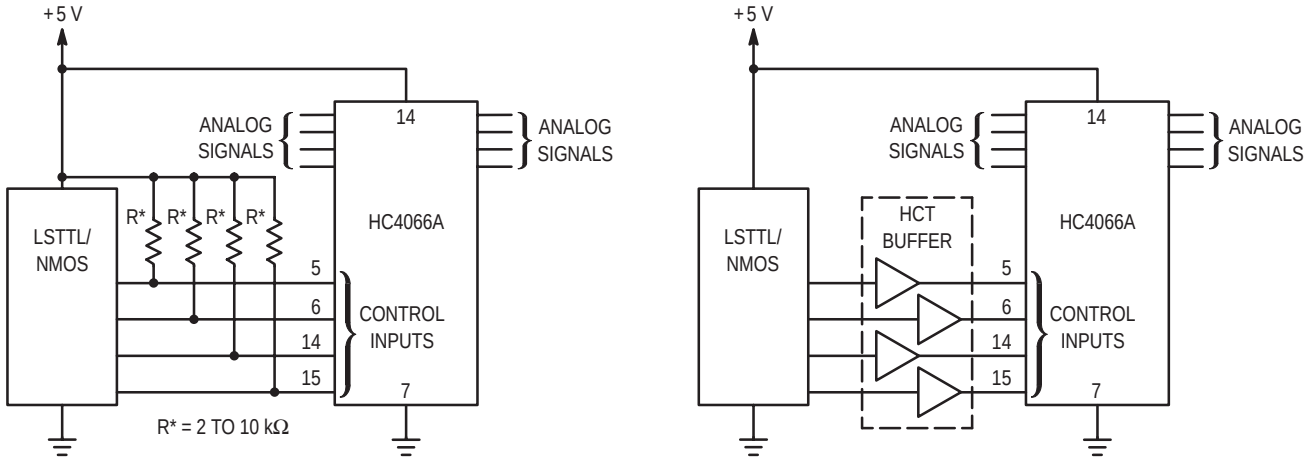


Figure 17. Transient Suppressor Application



a. Using Pull-Up Resistors **b. Using HCT Buffer**

Figure 18. LSTTL/NMOS to HCMOS Interface

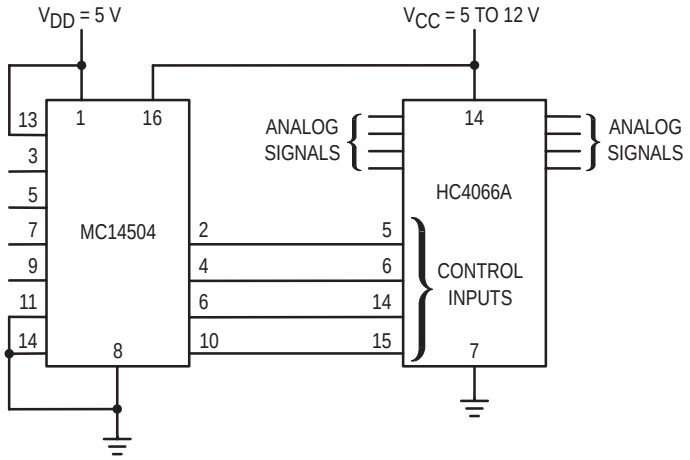


Figure 19. TTL/NMOS–to–CMOS Level Converter Analog Signal Peak–to–Peak Greater than 5 V (Also see HC4316A)

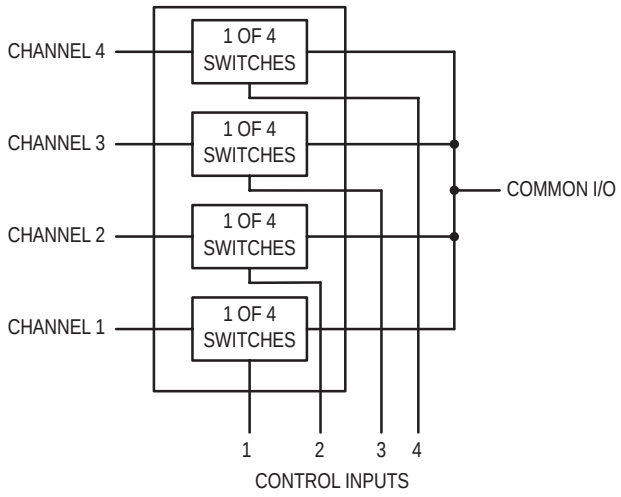


Figure 20. 4–Input Multiplexer

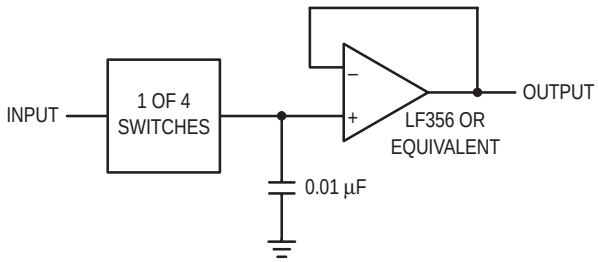


Figure 21. Sample/Hold Amplifier

MC74HC4316A

Product Preview

Quad Analog Switch/ Multiplexer/Demultiplexer with Separate Analog and Digital Power Supplies

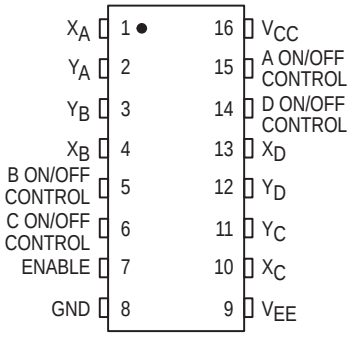
High–Performance Silicon–Gate CMOS

The MC74HC4316A utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF–channel leakage current. This bilateral switch/multiplexer/ demultiplexer controls analog and digital voltages that may vary across the full analog power–supply range (from V_{CC} to V_{EE}).

The HC4316A is similar in function to the metal–gate CMOS MC14016 and MC14066, and to the High–Speed CMOS HC4066A. Each device has four independent switches. The device control and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The device has been designed so that the ON resistances (R_{ON}) are much more linear over input voltage than R_{ON} of metal–gate CMOS analog switches. Logic–level translators are provided so that the On/Off Control and Enable logic–level voltages need only be V_{CC} and GND, while the switch is passing signals ranging between V_{CC} and V_{EE}. When the Enable pin (active–low) is high, all four analog switches are turned off.

- Logic–Level Translator for On/Off Control and Enable Inputs
- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Diode Protection on All Inputs/Outputs
- Analog Power–Supply Voltage Range ($V_{CC} – V_{EE}$) = 2.0 to 12.0 Volts
- Digital (Control) Power–Supply Voltage Range (V_{CC} – GND) = 2.0 to 6.0 Volts, Independent of V_{EE}
- Improved Linearity of ON Resistance
- Chip Complexity: 66 FETs or 16.5 Equivalent Gates

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		State of Analog Switch
Enable	On/Off Control	
L	H	On
L	L	Off
H	X	Off

X = don't care

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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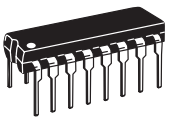
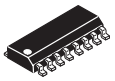
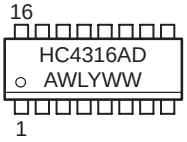
MARKING DIAGRAMS

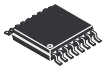


PDIP–16
P SUFFIX
CASE 648

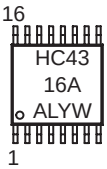


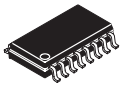
SOIC–16
D SUFFIX
CASE 751B



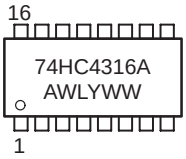


TSSOP–16
DT SUFFIX
CASE 948F





SOEIAJ–16
F SUFFIX
CASE 966



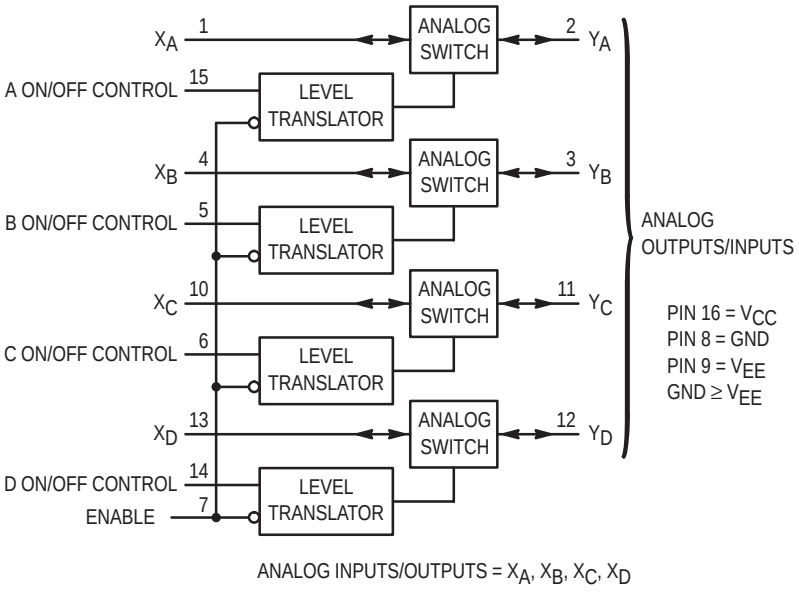
A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74HC4316AN	PDIP–16	2000 / Box
MC74HC4316AD	SOIC–16	48 / Rail
MC74HC4316ADR2	SOIC–16	2500 / Reel
MC74HC4316ADT	TSSOP–16	96 / Rail
MC74HC4316ADTR2	TSSOP–16	2500 / Reel
MC74HC4316AF	SOEIAJ–14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

LOGIC DIAGRAM



ANALOG INPUTS/OUTPUTS = X_A, X_B, X_C, X_D

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Ref. to GND) (Ref. to V_{EE})	– 0.5 to + 7.0 – 0.5 to + 14.0	V
V_{EE}	Negative DC Supply Voltage (Ref. to GND)	– 7.0 to + 0.5	V
V_{IS}	Analog Input Voltage	V_{EE} – 0.5 to V_{CC} + 0.5	V
V_{in}	DC Input Voltage (Ref. to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current Into or Out of Any Pin	± 25	mA
P_D	Power Dissipation in Still Air Plastic DIP† EIAJ/SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
EIAJ/SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Ref. to GND)		2.0	6.0	V
V_{EE}	Negative DC Supply Voltage (Ref. to GND)		– 6.0	GND	V
V_{IS}	Analog Input Voltage		V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Ref. to GND)		GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		—	1.2	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Control or Enable Inputs) (Figure 10)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

*For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) V_{EE} = GND Except Where Noted

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Voltage, Control or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Voltage, Control or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
I_{in}	Maximum Input Leakage Current, Control or Enable Inputs	V_{in} = V_{CC} or GND V_{EE} = – 6.0 V	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND V_{IO} = 0 V V_{EE} = GND V_{EE} = – 6.0	 6.0 6.0	 2 4	 20 40	 40 160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to V_{EE})

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit			Unit
					– 55 to 25°C	≤ 85°C	≤ 125°C	
R_{on}	Maximum "ON" Resistance	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ to V_{EE} $I_S \leq 2.0$ mA (Figures 1, 2)	2.0* 4 5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	— 160 90 90	— 200 110 110	— 240 130 130	Ω
		$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or V_{EE} (Endpoints) $I_S \leq 2.0$ mA (Figures 1, 2)	2.0 4.5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	— 90 70 70	— 115 90 90	— 140 105 105	
ΔR_{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IH}$ $V_{IS} = 1/2\ (V_{CC} - V_{EE})$ $I_S \leq 2.0$ mA	2.0 4.5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	— 20 15 15	— 25 20 20	— 30 25 25	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ $V_{IO} = V_{CC}$ or V_{EE} Switch Off (Figure 3)	6.0	– 6.0	0.1	0.5	1.0	μA
I_{on}	Maximum On–Channel Leakage Current, Any One Channel	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or V_{EE} (Figure 4)	6.0	– 6.0	0.1	0.5	1.0	μA

*At supply voltage ($V_{CC} - V_{EE}$) approaching 2 V the analog switch–on resistance becomes extremely non–linear. Therefore, for low–voltage operation, it is recommended that these devices only be used to control digital signals.

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Control or Enable $t_r = t_f$ = 6 ns, V_{EE} = GND)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0 4.5 6.0	40 6 5	50 8 7	60 9 8	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Control or Enable to Analog Output (Figures 10 and 11)	2.0 4.5 6.0	130 40 30	160 50 40	200 60 50	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Control or Enable to Analog Output (Figures 10 and 11)	2.0 4.5 6.0	140 40 30	175 50 40	250 60 50	ns
C	Maximum Capacitance — ON/OFF Control and Enable Inputs	—	10	10	10	pF
	Control Input = GND Analog I/O Feedthrough	 — —	 35 1.0	 35 1.0	 35 1.0	

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Switch) (Figure 13)*	15	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Limit* 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 5)	f_{in} = 1 MHz Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{OS} Increase f_{in} Frequency Until dB Meter Reads – 3 dB R_L = 50 Ω, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	150 160 160	MHz
—	Off–Channel Feedthrough Isolation (Figure 6)	f_{in} ≡ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 50 – 50 – 50	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 40 – 40 – 40	
—	Feedthrough Noise, Control to Switch (Figure 7)	V_{in} ≤ 1 MHz Square Wave (t_r = t_f = 6 ns) Adjust R_L at Setup so that I_S = 0 A R_L = 600 Ω, C_L = 50 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	60 130 200	mV_{PP}
		R_L = 10 kΩ, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	30 65 100	
—	Crosstalk Between Any Two Switches (Figure 12)	f_{in} ≡ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 70 – 70 – 70	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 80 – 80 – 80	
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1 kHz, R_L = 10 kΩ, C_L = 50 pF $THD = THD_{Measured} - THD_{Source}$ V_{IS} = 4.0 V_{PP} sine wave V_{IS} = 8.0 V_{PP} sine wave V_{IS} = 11.0 V_{PP} sine wave	 2.25 4.50 6.00	 – 2.25 – 4.50 – 6.00	 0.10 0.06 0.04	%

*Limits not tested. Determined by design and verified by qualification.

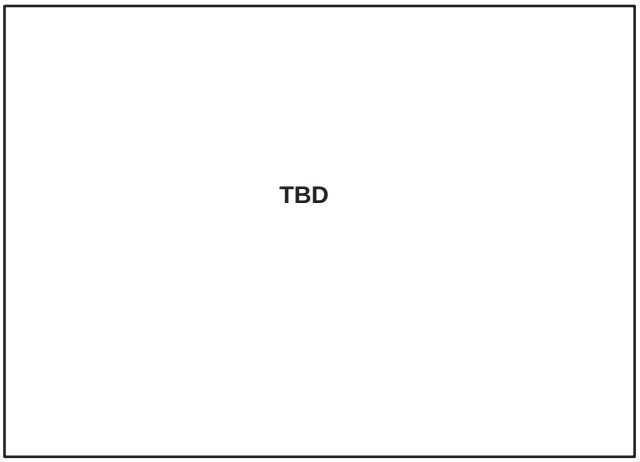


Figure 1a. Typical On Resistance,
$V_{CC} - V_{EE}$ = 2.0 V

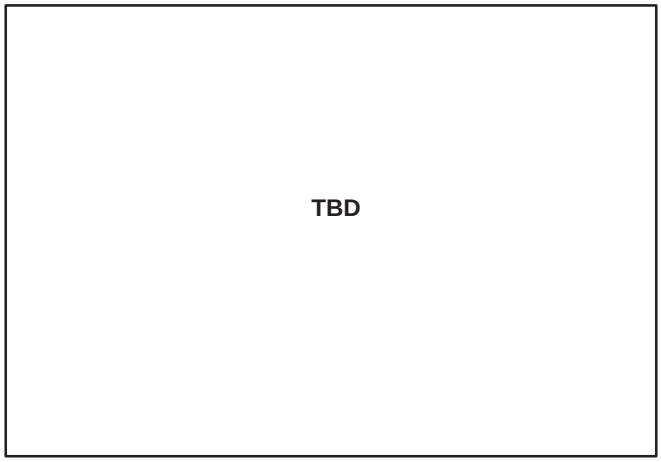


Figure 1b. Typical On Resistance,
$V_{CC} - V_{EE}$ = 4.5 V

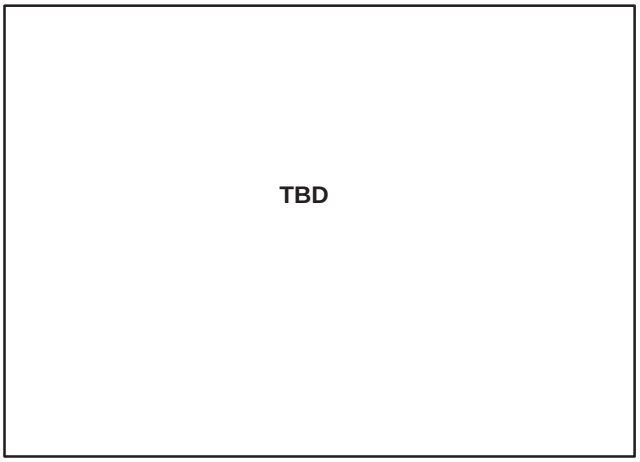


Figure 1c. Typical On Resistance,
$V_{CC} - V_{EE}$ = 6.0 V

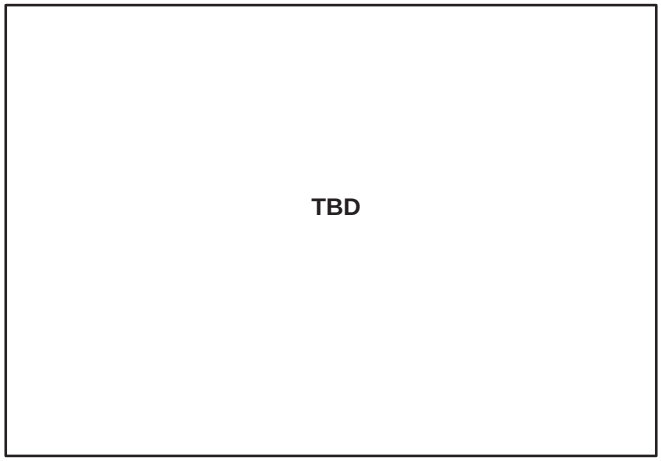


Figure 1d. Typical On Resistance,
$V_{CC} - V_{EE}$ = 9.0 V

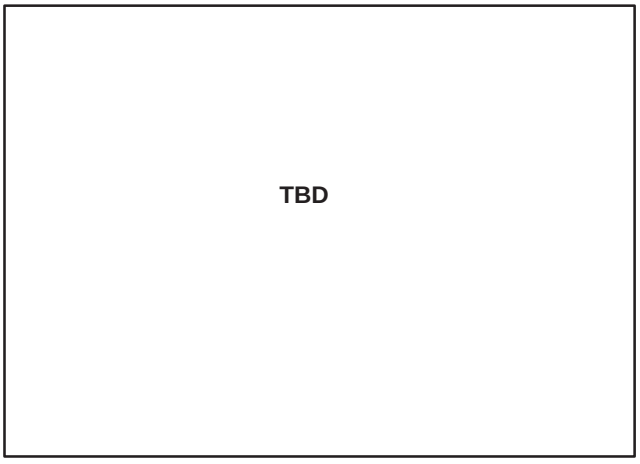


Figure 1e. Typical On Resistance,
$V_{CC} - V_{EE}$ = 12.0 V

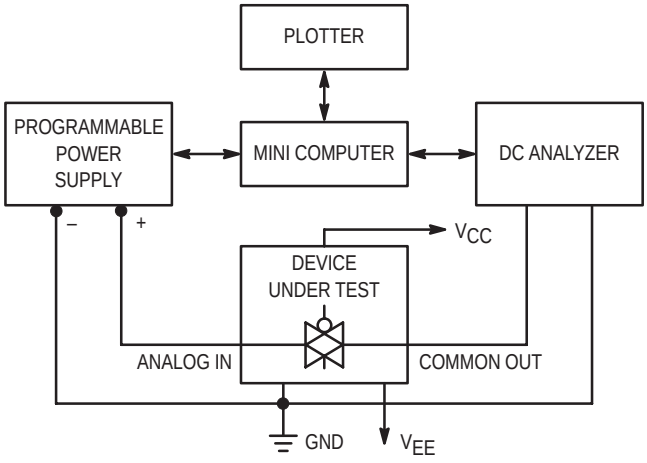


Figure 2. On Resistance Test Set–Up

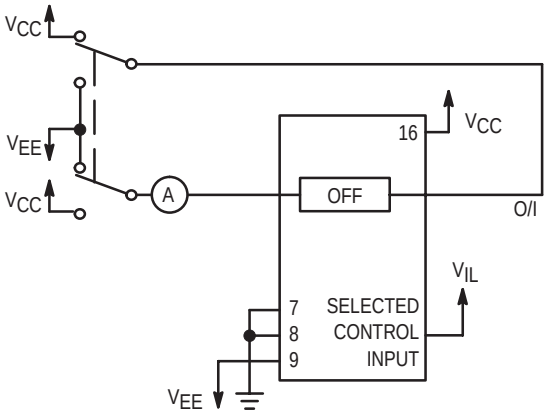


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

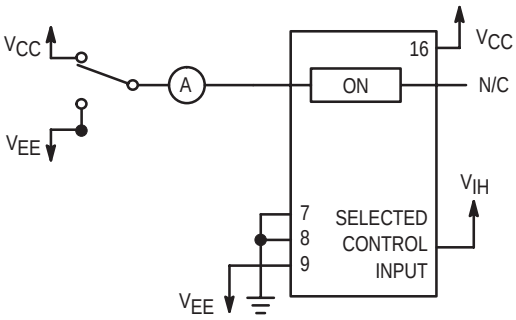
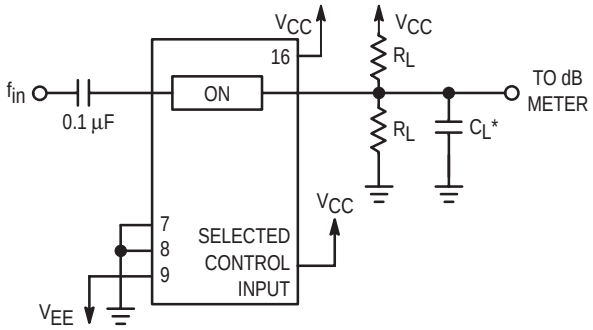
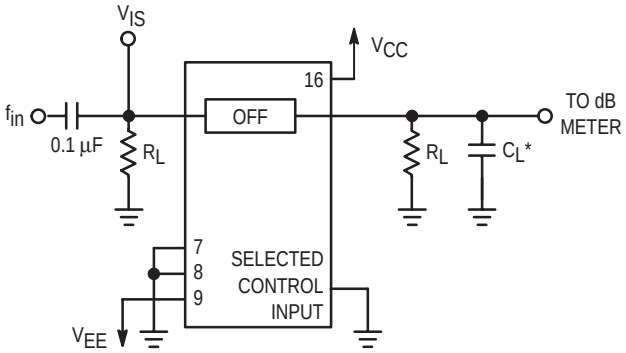


Figure 4. Maximum On Channel Leakage Current, Test Set–Up



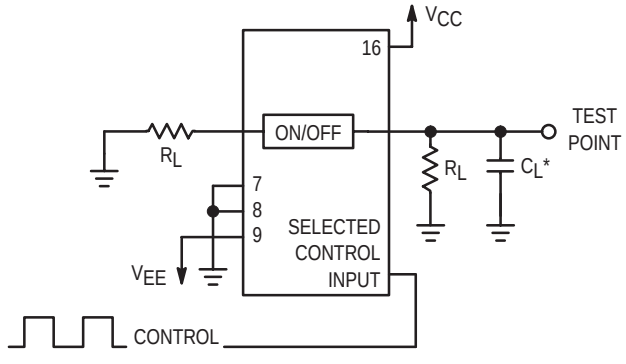
*Includes all probe and jig capacitance.

Figure 5. Maximum On–Channel Bandwidth Test Set–Up



*Includes all probe and jig capacitance.

Figure 6. Off–Channel Feedthrough Isolation, Test Set–Up



*Includes all probe and jig capacitance.

Figure 7. Feedthrough Noise, Control to Analog Out, Test Set–Up

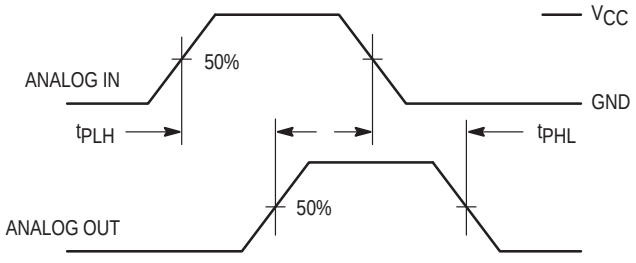
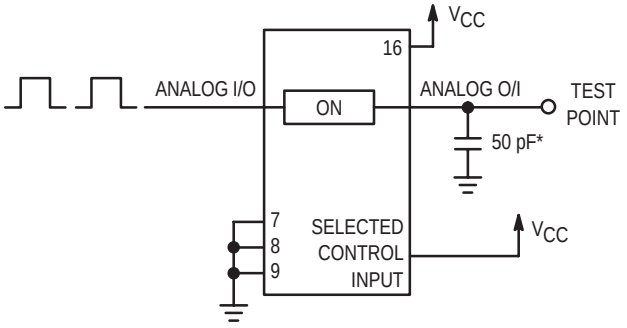


Figure 8. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set–Up

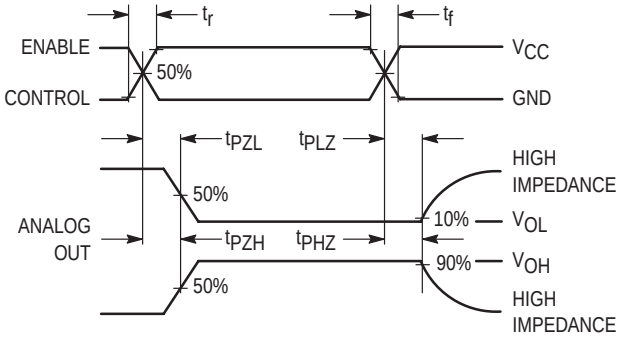
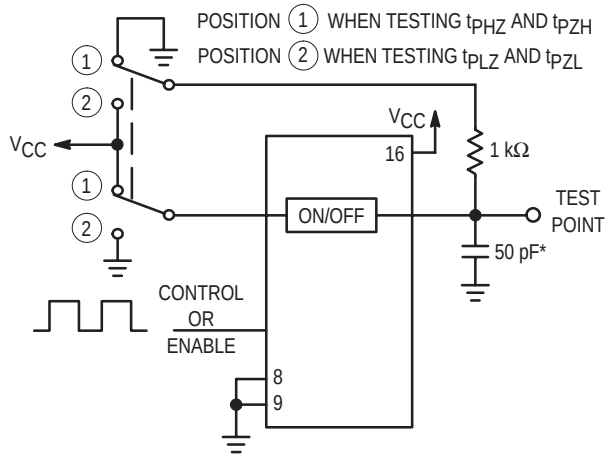
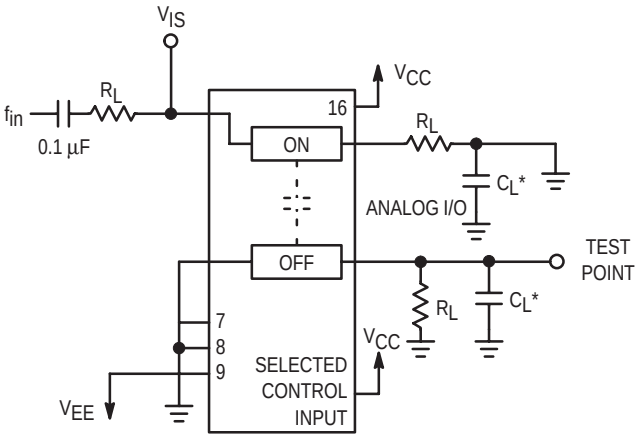


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set–Up



*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set–Up (Adjacent Channels Used)

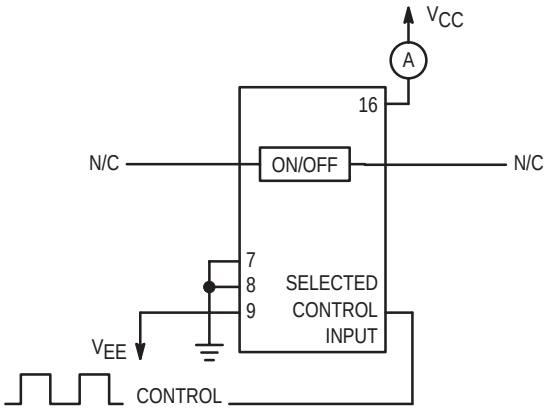
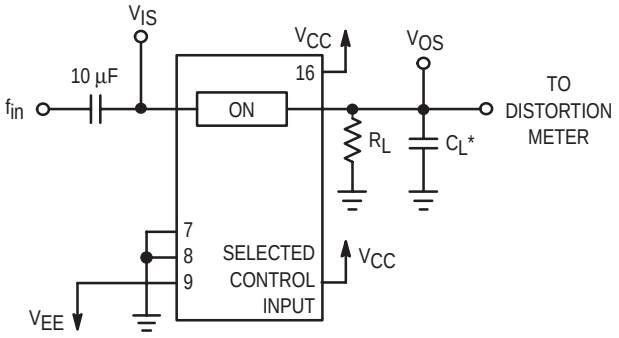


Figure 13. Power Dissipation Capacitance Test Set–Up



*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set–Up

APPLICATIONS INFORMATION

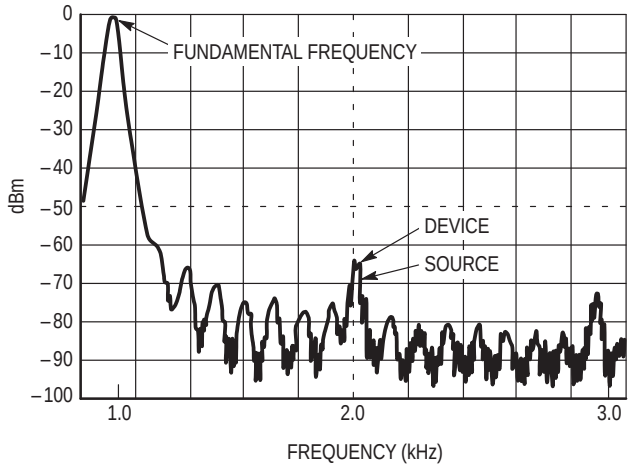


Figure 15. Plot, Harmonic Distortion

The Enable and Control pins should be at V_{CC} or GND logic levels, V_{CC} being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to V_{CC} or V_{EE} through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below V_{EE}. In the example below, the difference between V_{CC} and V_{EE} is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak–to–peak can be controlled.

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure 17. These diodes should be small signal, fast turn–on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the Dx diodes with Mosorbs (Mosorb™ is an acronym for high current surge protectors). Mosorbs are fast turn–on devices ideally suited for precise dc protection with no inherent wear out mechanism.

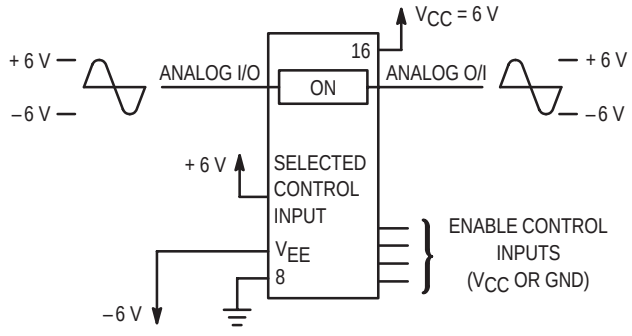


Figure 16.

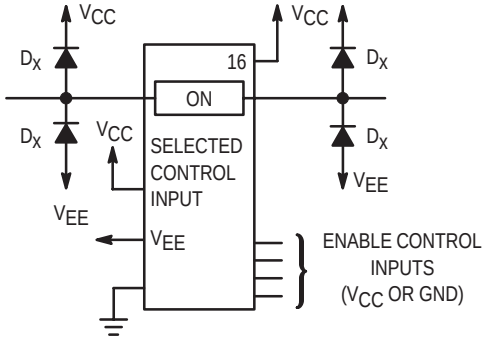
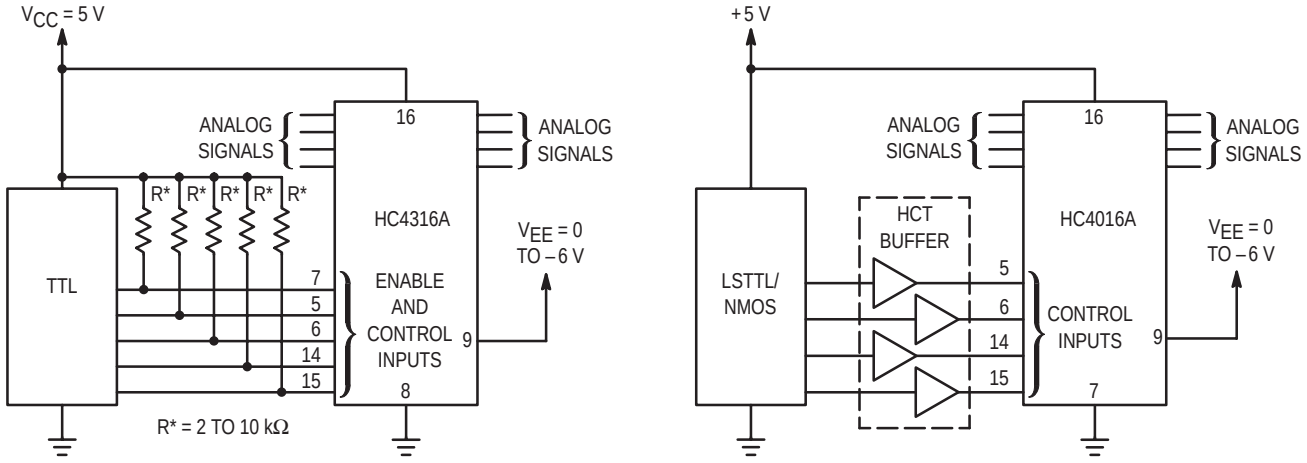


Figure 17. Transient Suppressor Application



a. Using Pull–Up Resistors **b. Using HCT Buffer**

Figure 18. LSTTL/NMOS to HCMOS Interface

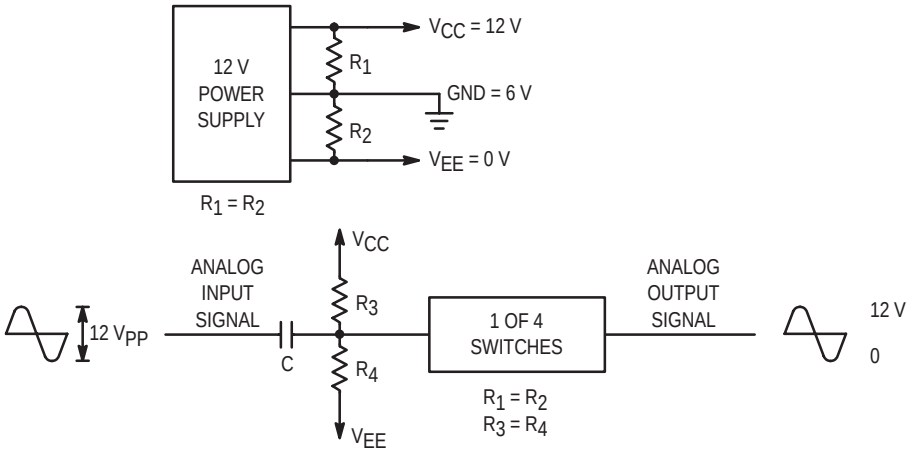


Figure 19. Switching a 0–to–12 V Signal Using a Single Power Supply (GND ≠ 0 V)

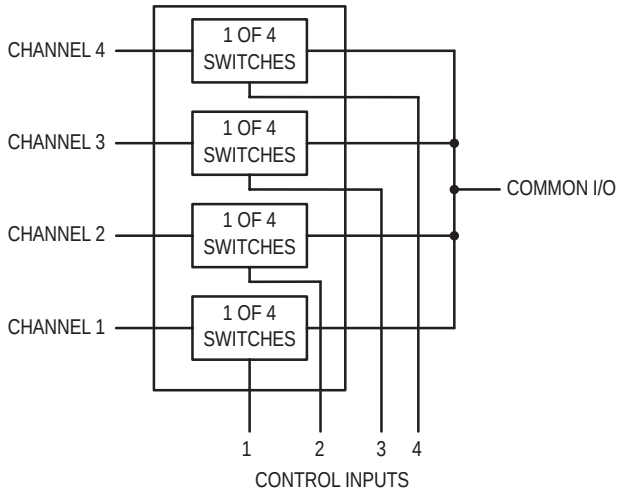


Figure 20. 4–Input Multiplexer

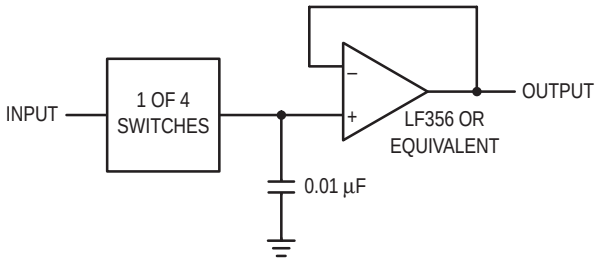


Figure 21. Sample/Hold Amplifier

MC74HC4851A, MC74HC4852A

Analog Multiplexers/ Demultiplexers with Injection Current Effect Control

Automotive Customized

These devices are pin compatible to standard HC405x and MC1405xB analog mux/demux devices, but feature injection current effect control. This makes them especially suited for usage in automotive applications where voltages in excess of normal logic voltage are common.

The injection current effect control allows signals at disabled analog input channels to exceed the supply voltage range without affecting the signal of the enabled analog channel. This eliminates the need for external diode/ resistor networks typically used to keep the analog channel signals within the supply voltage range.

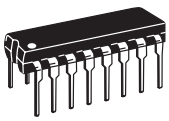
The devices utilize low power silicon gate CMOS technology. The Channel Select and Enable inputs are compatible with standard CMOS outputs.

- Injection Current Cross–Coupling Less than 1mV/mA (See Figure 9)
- Pin Compatible to HC405X and MC1405XB Devices
- Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- In Compliance With the Requirements of JEDEC Standard No. 7A
- Chip Complexity: 154 FETs or 36 Equivalent Gates

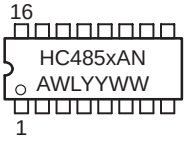
ON Semiconductor

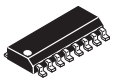
http://onsemi.com

MARKING DIAGRAMS

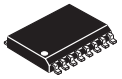


PDIP–16
N SUFFIX
CASE 648



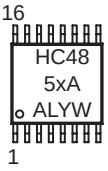


SOIC–16
D SUFFIX
CASE 751B



SOIC–16 WIDE
DW SUFFIX
CASE 751G

TSSOP–16
DT SUFFIX
CASE 948F



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 96 of this data sheet.

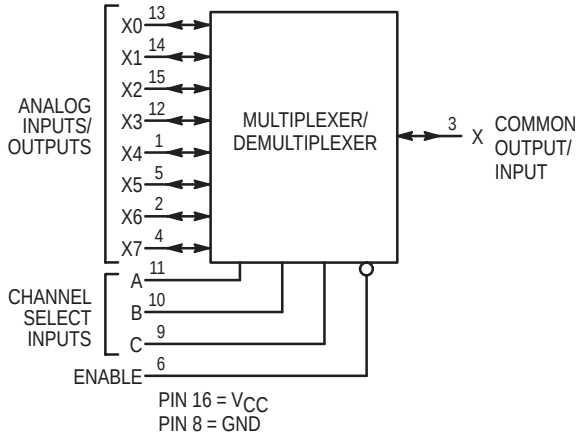


Figure 1. MC74HC4851A Logic Diagram
Single–Pole, 8–Position Plus Common Off

FUNCTION TABLE – MC74HC4851A

Control Inputs				
	Select			
Enable	C	B	A	ON Channels
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

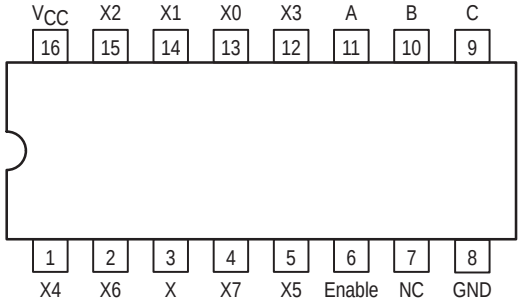


Figure 2. MC74HC4851A 16–Lead Pinout (Top View)

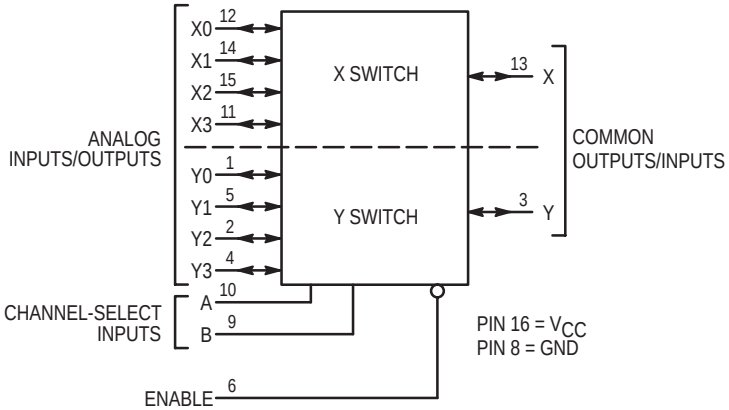


Figure 3. MC74HC4852A Logic Diagram
Double–Pole, 4–Position Plus Common Off

FUNCTION TABLE – MC74HC4852A

Control Inputs			
	Select		
Enable	B	A	ON Channels
L	L	L	Y0 X0
L	L	H	Y1 X1
L	H	L	Y2 X2
L	H	H	Y3 X3
H	X	X	NONE

X = Don't Care

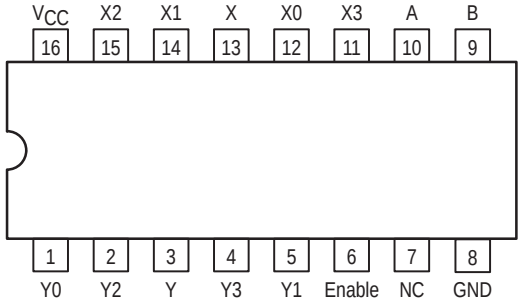


Figure 4. MC74HC4852A 16–Lead Pinout (Top View)

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Any Pin) (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin	± 25	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}	DC Input Voltage (Any Pin) (Referenced to GND)		GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		0.0	1.2	V
T_A	Operating Temperature Range, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

*For voltage drops across switch greater than 1.2V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) V_{EE} = GND, Except Where Noted

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
I_{in}	Maximum Input Leakage Current on Digital Pins (Enable/A/B/C)	V_{in} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in(digital)}$ = V_{CC} or GND $V_{in(analog)}$ = GND	6.0	2	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

DC CHARACTERISTICS — Analog Section

Symbol	Parameter	Condition	V_{CC}	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
R_{on}	Maximum "ON" Resistance	V_{in} = V_{IL} or V_{IH}; V_{IS} = V_{CC} to GND; I_S ≤ 2.0 mA	2.0 3.0 4.5 6.0	1700 1100 550 400	1750 1200 650 500	1800 1300 750 600	Ω
ΔR_{on}	Delta "ON" Resistance	V_{in} = V_{IL} or V_{IH}; V_{IS} = V_{CC}/2 I_S ≤ 2.0 mA	2.0 3.0 4.5 6.0	300 160 80 60	400 200 100 80	500 240 120 100	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel Common Channel	V_{in} = V_{CC} or GND	6.0	±0.1 ±0.2	±0.5 ±2.0	±1.0 ±4.0	μA
I_{on}	Maximum On–Channel Leakage Channel–to–Channel	V_{in} = V_{CC} or GND	6.0	±0.2	±2.0	±4.0	μA

AC CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V_{CC}	–55 to 25°C	≤85°C	≤125°C	Unit
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Analog Input to Analog Output	2.0 3.0 4.5 6.0	160 80 40 30	180 90 45 35	200 100 50 40	ns
t_{PHL}, $t_{PHZ,PZH}$ t_{PLH}, $t_{PLZ,PZL}$	Maximum Propagation Delay, Enable or Channel–Select to Analog Output	2.0 3.0 4.5 6.0	260 160 80 60	280 180 90 70	300 200 100 80	ns
C_{in}	Maximum Input Capacitance Digital Pins (All Switches Off) Any Single Analog Pin (All Switches Off) Common Analog Pin		10 35 130	10 35 130	10 35 130	pF
C_{PD}	Power Dissipation Capacitance Typical	5.0	20			pF

INJECTION CURRENT COUPLING SPECIFICATIONS (V_{CC} = 5V, T_A = –55°C to +125°C)

Symbol	Parameter	Typ	Max	Unit	Condition
$V\Delta_{out}$	Maximum Shift of Output Voltage of Enabled Analog Channel	0.1 1.0 0.5 5.0	1.0 5.0 2.0 20	mV	I_{in}* ≤ 1mA, R_S ≤ 3,9kΩ I_{in}* ≤ 10mA, R_S ≤ 3,9kΩ I_{in}* ≤ 1mA, R_S ≤ 20kΩ I_{in}* ≤ 10mA, R_S ≤ 20kΩ

* I_{in} = Total current injected into all disabled channels.

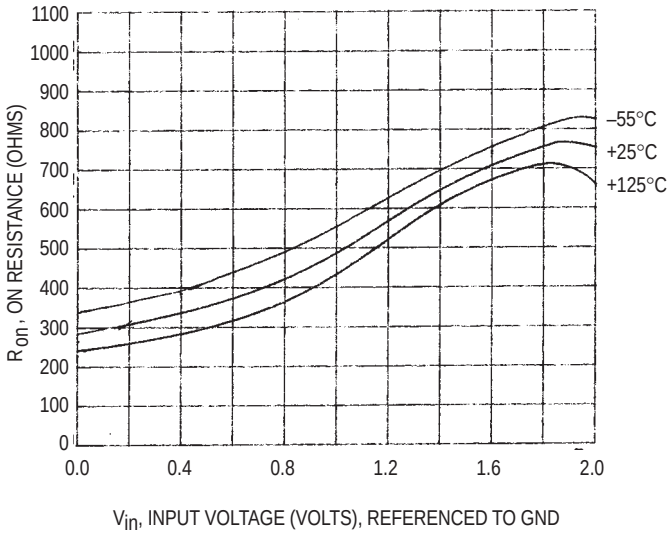


Figure 5. Typical On Resistance V_{CC} = 2V

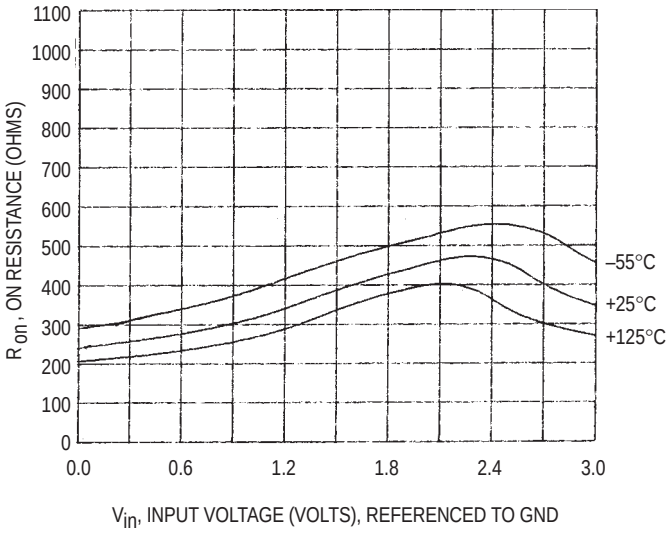


Figure 6. Typical On Resistance V_{CC} = 3V

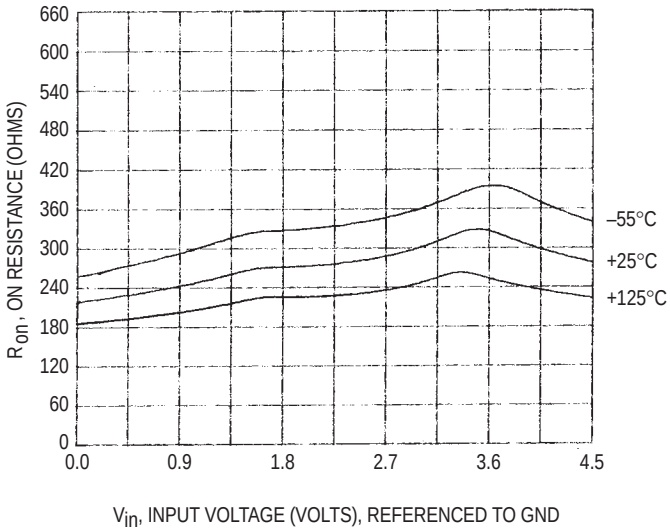


Figure 7. Typical On Resistance V_{CC} = 4.5V

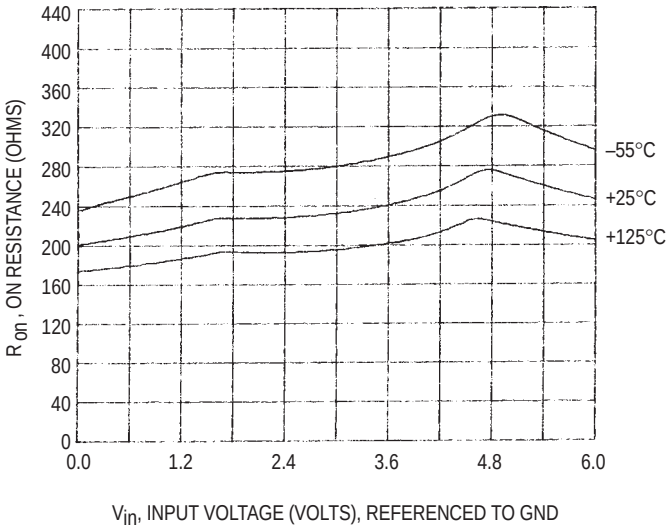


Figure 8. Typical On Resistance V_{CC} = 6V

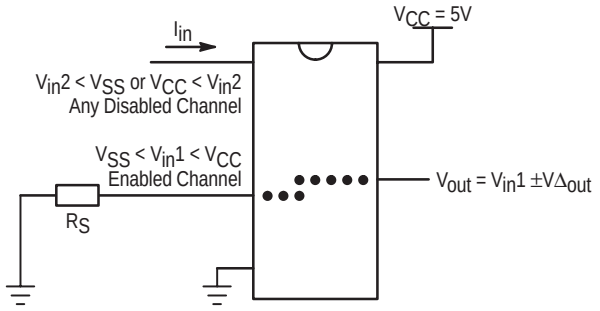


Figure 9. Injection Current Coupling Specification

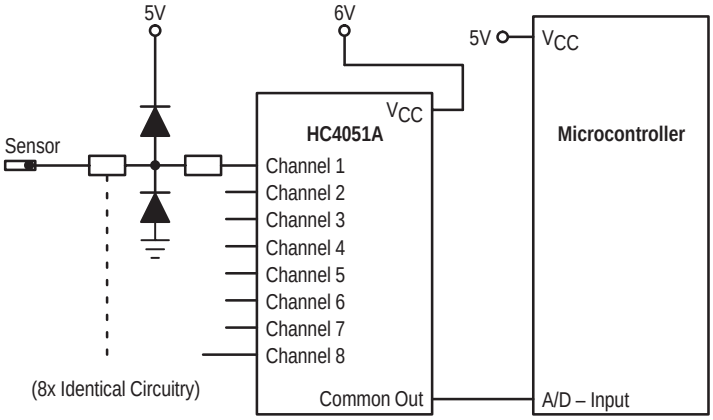


Figure 10. Actual Technology
Requires 32 passive components and one extra 6V regulator
to suppress injection current into a standard HC4051 multiplexer

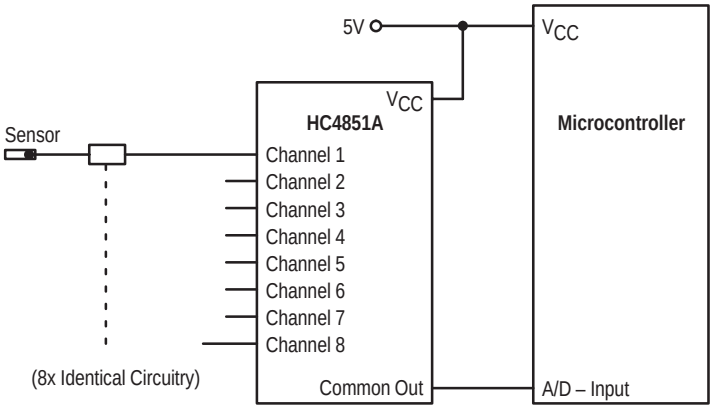


Figure 11. MC74HC4851A Solution
Solution by applying the HC4851A multiplexer

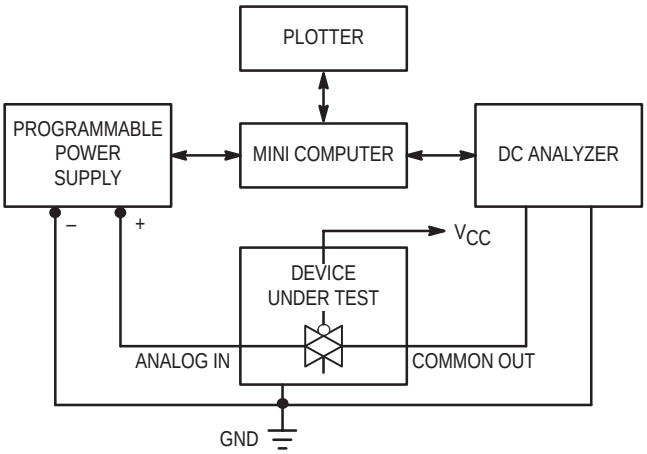


Figure 12. On Resistance Test Set–Up

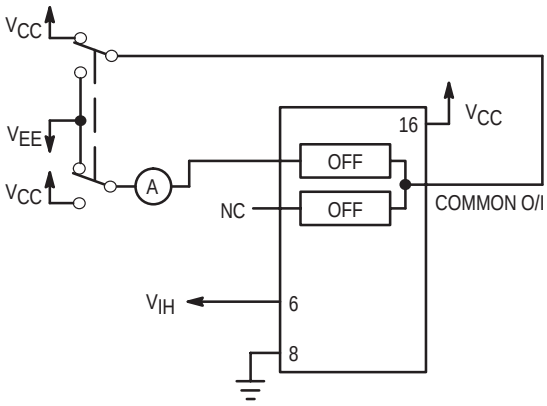


Figure 13. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

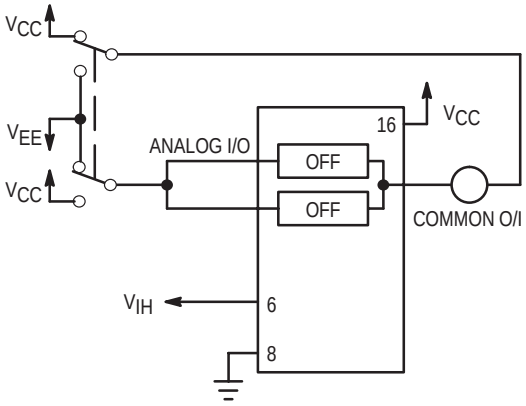


Figure 14. Maximum Off Channel Leakage Current, Common Channel, Test Set–Up

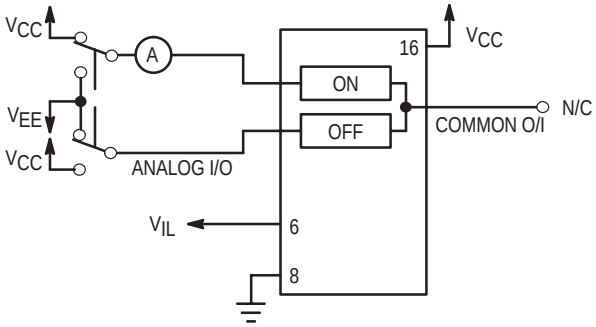


Figure 15. Maximum On Channel Leakage Current, Channel to Channel, Test Set–Up

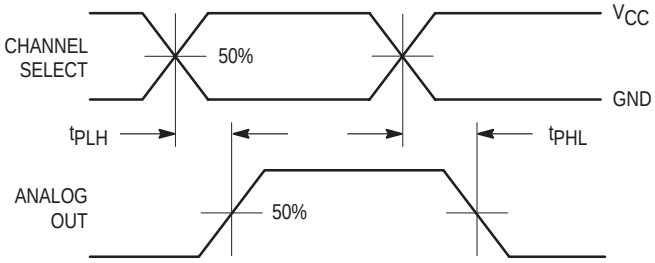
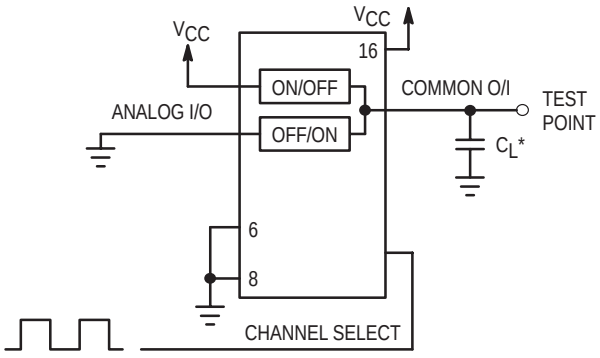


Figure 16. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 17. Propagation Delay, Test Set–Up Channel Select to Analog Out

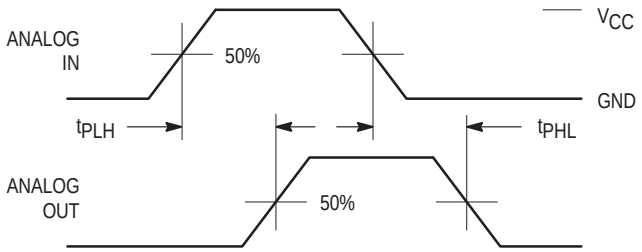
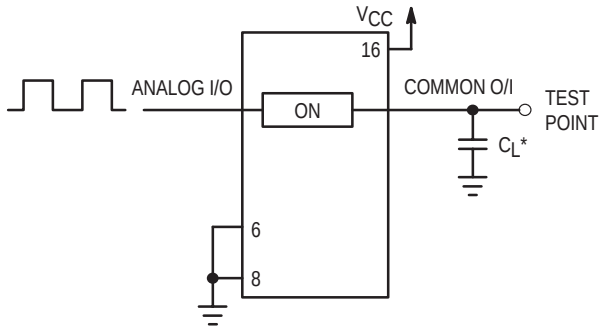


Figure 18. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 19. Propagation Delay, Test Set–Up Analog In to Analog Out

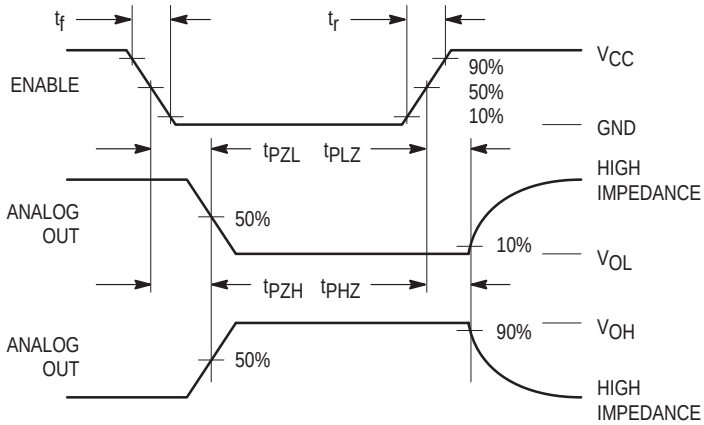


Figure 20. Propagation Delays, Enable to Analog Out

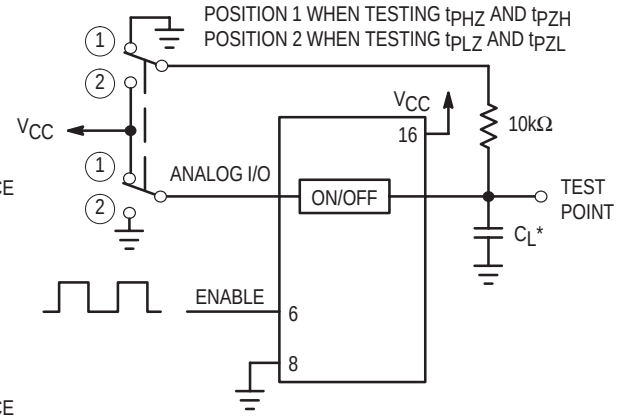


Figure 21. Propagation Delay, Test Set–Up Enable to Analog Out

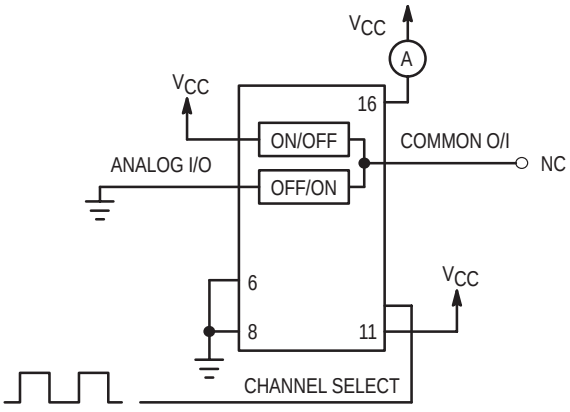


Figure 22. Power Dissipation Capacitance, Test Set–Up

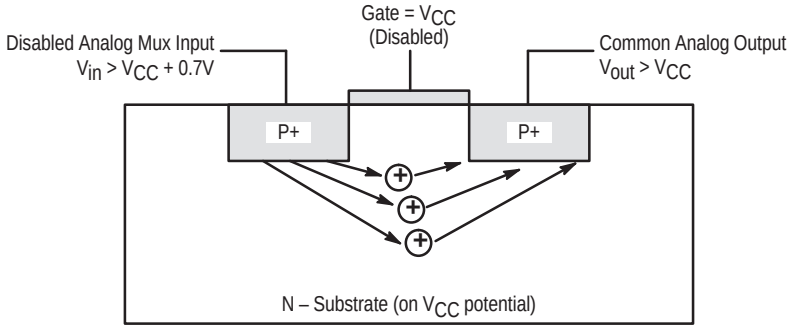


Figure 23. Diagram of Bipolar Coupling Mechanism
Appears if V_{in} exceeds V_{CC}, driving injection current into the substrate

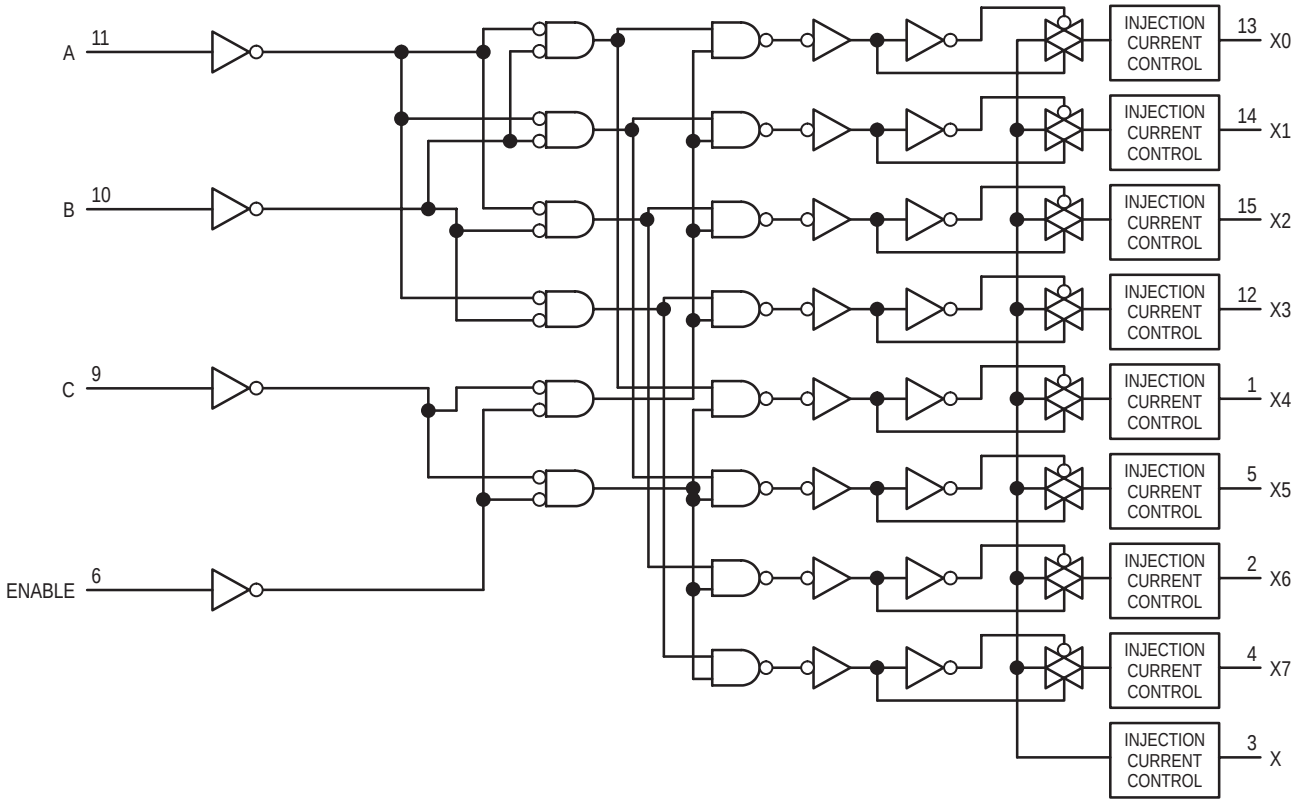


Figure 24. Function Diagram, HC4851A

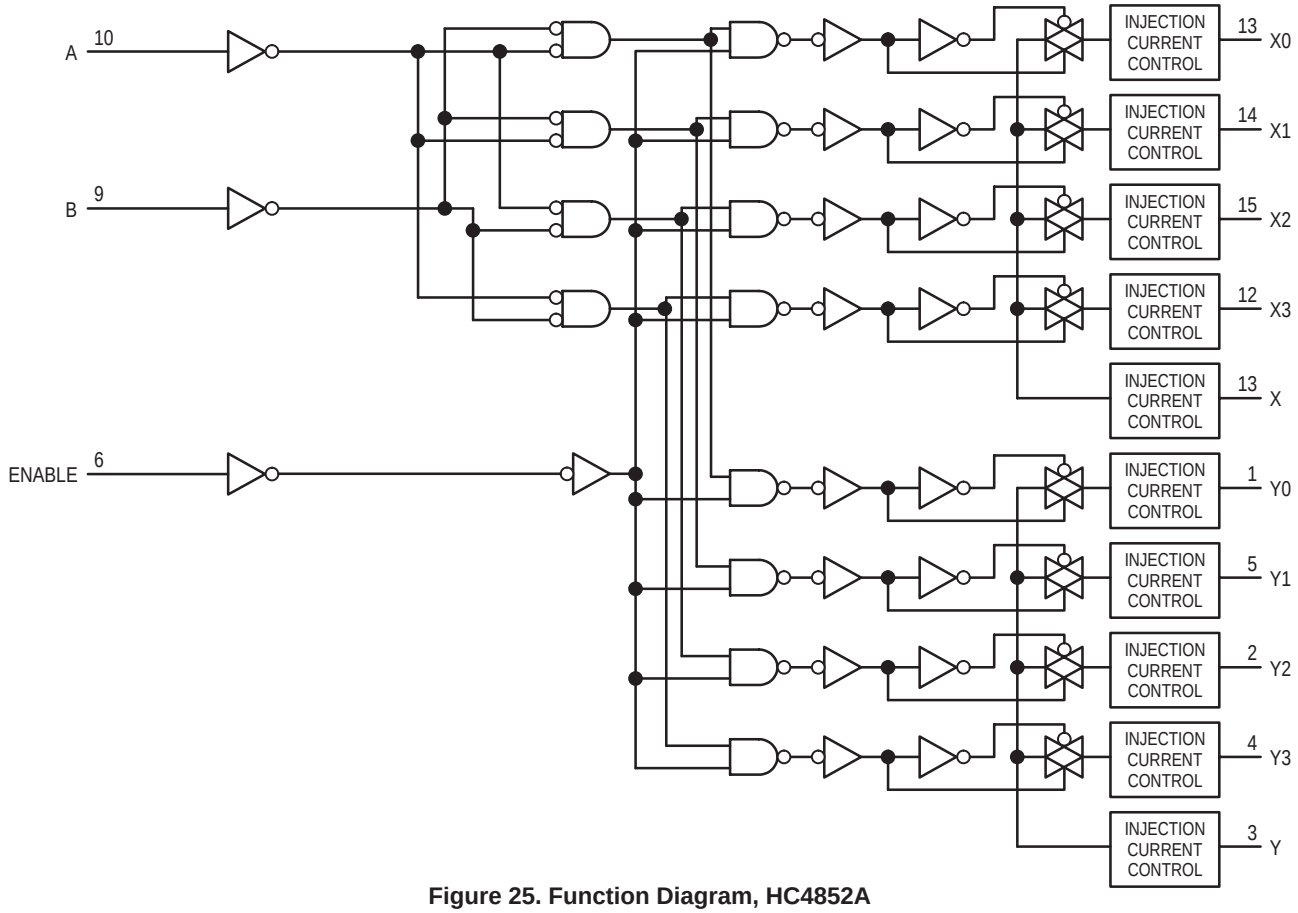


Figure 25. Function Diagram, HC4852A

ORDERING & SHIPPING INFORMATION

Device	Package	Shipping
MC74HC4851AN	PDIP–16	500 Units / Unit Pak
MC74HC4851AD	SOIC–16	48 Units / Rail
MC74HC4851ADR2	SOIC–16	2500 Units / Tape & Reel
MC74HC4851ADW	SOIC–16 WIDE	48 Units / Rail
MC74HC4851ADWR2	SOIC–16 WIDE	1000 Units / Tape & Reel
MC74HC4851ADT	TSSOP–16	96 Units / Rail
MC74HC4851ADTR2	TSSOP–16	2500 Units / Tape & Reel
MC74HC4852AN	PDIP–16	500 Units / Unit Pak
MC74HC4852AD	SOIC–16	48 Units / Rail
MC74HC4852ADR2	SOIC–16	2500 Units / Tape & Reel
MC74HC4852ADW	SOIC–16 WIDE	48 Units / Rail
MC74HC4852ADWR2	SOIC–16 WIDE	1000 Units / Tape & Reel
MC74HC4852ADT	TSSOP–16	96 Units / Rail
MC74HC4852ADTR2	TSSOP–16	2500 Units / Tape & Reel

MC74VHC4051, MC74VHC4052, MC74VHC4053

Analog Multiplexers / Demultiplexers

High–Performance Silicon–Gate CMOS

The MC74VHC4051, MC74VHC4052 and MC74VHC4053 utilize silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The VHC4051, VHC4052 and VHC4053 are identical in pinout to the high–speed HC4051A, HC4052A and HC4053A, and the metal–gate MC14051B, MC14052B and MC14053B. The Channel–Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel–Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors they are compatible with LSTTL outputs.

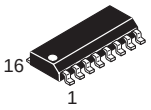
These devices have been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal–gate CMOS analog switches.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ($V_{CC} – V_{EE}$) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range ($V_{CC} – GND$) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal–Gate Counterparts
- Low Noise
- Chip Complexity: VHC4051 — 184 FETs or 46 Equivalent Gates
  VHC4052 — 168 FETs or 42 Equivalent Gates
  VHC4053 — 156 FETs or 39 Equivalent Gates

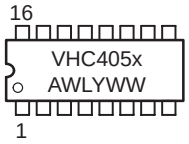
ON Semiconductor

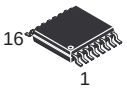
http://onsemi.com

MARKING DIAGRAMS

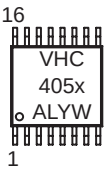


SO–16
D SUFFIX
CASE 751B





TSSOP–16
DT SUFFIX
CASE 948F

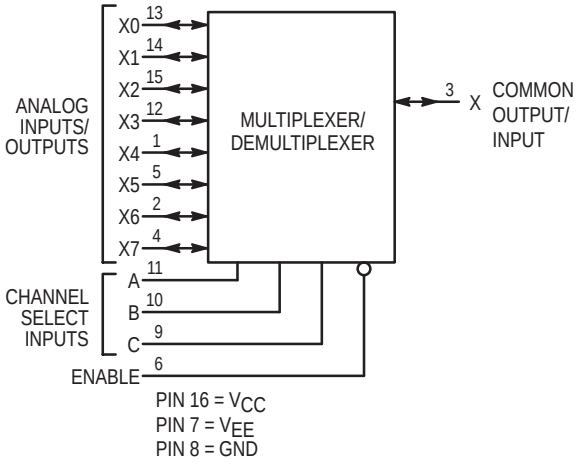


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 110 of this data sheet.

LOGIC DIAGRAM
MC74VHC4051
Single–Pole, 8–Position Plus Common Off

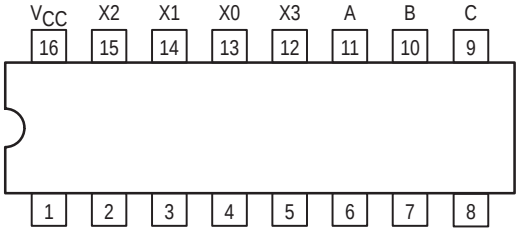


FUNCTION TABLE – MC74VHC4051

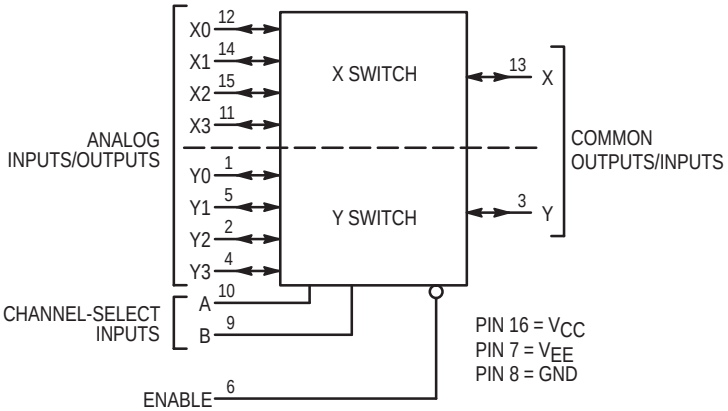
Control Inputs				
	Select			
Enable	C	B	A	ON Channels
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

X = Don't Care

Pinout: MC74VHC4051 (Top View)



LOGIC DIAGRAM
MC74VHC4052
Double–Pole, 4–Position Plus Common Off

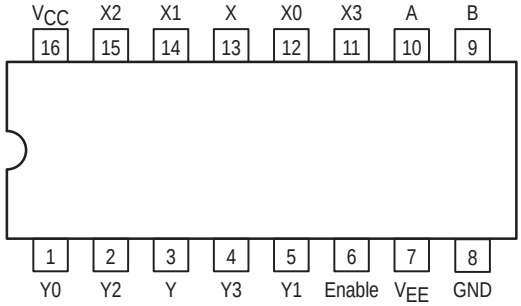


FUNCTION TABLE – MC74VHC4052

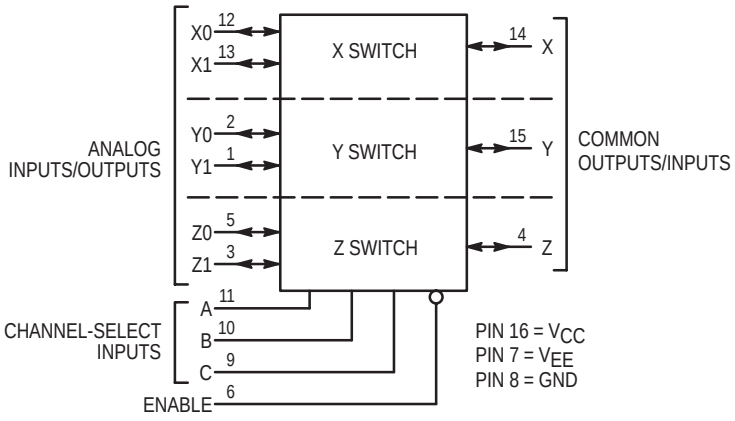
Control Inputs				
	Select			
Enable	B	A	ON Channels	
L	L	L	Y0	X0
L	L	H	Y1	X1
L	H	L	Y2	X2
L	H	H	Y3	X3
H	X	X	NONE	

X = Don't Care

Pinout: MC74VHC4052 (Top View)



LOGIC DIAGRAM
MC74VHC4053
Triple Single–Pole, Double–Position Plus Common Off



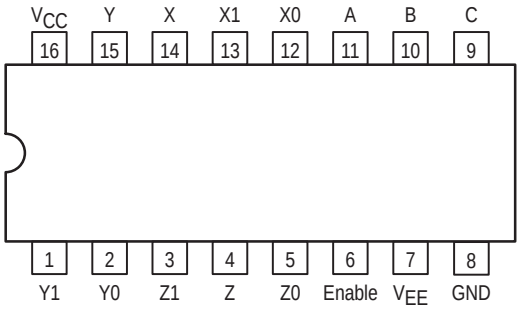
NOTE: This device allows independent control of each switch. Channel–Select Input A controls the X–Switch, Input B controls the Y–Switch and Input C controls the Z–Switch

FUNCTION TABLE – MC74VHC4053

Control Inputs						
	Select			ON Channels		
Enable	C	B	A			
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	NONE		

X = Don’t Care

Pinout: MC74VHC4053 (Top View)



MAXIMUM RATINGS*

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage	(Referenced to GND) (Referenced to V_{EE})	– 0.5 to + 7.0 – 0.5 to + 14.0	V
V_{EE}	Negative DC Supply Voltage (Referenced to GND)		– 7.0 to + 5.0	V
V_{IS}	Analog Input Voltage		V_{EE} – 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)		– 0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin		± 25	mA
P_D	Power Dissipation in Still Air,	SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range		– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	(Referenced to GND) (Referenced to V_{EE})	2.0 2.0	6.0 12.0	V
V_{EE}	Negative DC Supply Voltage, Output (Referenced to GND)		– 6.0	GND	V
V_{IS}	Analog Input Voltage		V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)		GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch			1.2	V
T_A	Operating Temperature Range, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 800 500 400	ns

*For voltage drops across switch greater than 1.2V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) V_{EE} = GND, Except Where Noted

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
I_{in}	Maximum Input Leakage Current, Channel–Select or Enable Inputs	V_{in} = V_{CC} or GND, V_{EE} = – 6.0 V	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and V_{IS} = V_{CC} or GND; V_{EE} = GND V_{IO} = 0 V V_{EE} = – 6.0	 6.0 6.0	 1 4	 10 40	 40 80	μA

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit			Unit
					– 55 to 25°C	≤ 85°C	≤ 125°C	
R_{on}	Maximum “ON” Resistance	V_{in} = V_{IL} or V_{IH} V_{IS} = V_{CC} to V_{EE} I_S ≤ 2.0 mA (Figures 1, 2)	3.0 4.5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	200 160 120 100	240 200 150 125	320 280 170 140	Ω
		V_{in} = V_{IL} or V_{IH} V_{IS} = V_{CC} or V_{EE} (Endpoints) I_S ≤ 2.0 mA (Figures 1, 2)	3.0 4.5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	150 110 90 80	180 140 120 100	230 190 140 115	
ΔR_{on}	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	V_{in} = V_{IL} or V_{IH} V_{IS} = 1/2 (V_{CC} – V_{EE}) I_S ≤ 2.0 mA	3.0 4.5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	40 20 10 10	50 25 15 12	80 40 18 14	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} – V_{EE}; Switch Off (Figure 3)	6.0	– 6.0	0.1	0.5	1.0	μA
	Maximum Off–Channel Leakage Current, Common Channel VHC4051 VHC4052 VHC4053	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} – V_{EE}; Switch Off (Figure 4)	6.0 6.0 6.0	– 6.0 – 6.0 – 6.0	0.2 0.1 0.1	2.0 1.0 1.0	4.0 2.0 2.0	
I_{on}	Maximum On–Channel Leakage Current, Channel–to–Channel VHC4051 VHC4052 VHC4053	V_{in} = V_{IL} or V_{IH}; Switch–to–Switch = V_{CC} – V_{EE}; (Figure 5)	6.0 6.0 6.0	– 6.0 – 6.0 – 6.0	0.2 0.1 0.1	2.0 1.0 1.0	4.0 2.0 2.0	μA

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Channel–Select to Analog Output (Figure 9)	2.0 3.0 4.5 6.0	270 90 59 45	320 110 79 65	350 125 85 75	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0 3.0 4.5 6.0	40 25 12 10	60 30 15 13	70 32 18 15	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 6.0	160 70 48 39	200 95 63 55	220 110 76 63	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 6.0	245 115 49 39	315 145 69 58	345 155 83 67	ns
C_{in}	Maximum Input Capacitance, Channel–Select or Enable Inputs		10	10	10	pF
$C_{I/O}$	Maximum Capacitance — Analog I/O		35	35	35	pF
	(All Switches Off) — Common O/I: VHC4051 VHC4052 VHC4053		130 80 50	130 80 50	130 80 50	
	Feedthrough		1.0	1.0	1.0	

			Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0 V	
C_{PD}	Power Dissipation Capacitance (Figure 13)*	VHC4051 VHC4052 VHC4053	45 80 45	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V_{CC} V	V_{EE} V	Limit* 25°C '51	Limit* 25°C '52	Limit* 25°C '53	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 6)	f_{in} = 1MHz Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{OS}; Increase f_{in} Frequency Until dB Meter Reads –3dB; R_L = 50Ω, C_L = 10pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	80 80 80	95 95 95	120 120 120	MHz
—	Off–Channel Feedthrough Isolation (Figure 7)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600Ω, C_L = 50pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	–50 –50 –50			dB
		f_{in} = 1.0MHz, R_L = 50Ω, C_L = 10pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	–40 –40 –40			
—	Feedthrough Noise. Channel–Select Input to Common I/O (Figure 8)	V_{in} ≤ 1MHz Square Wave (t_r = t_f = 6ns); Adjust R_L at Setup so that I_S = 0A; Enable = GND R_L = 600Ω, C_L = 50pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	25 105 135			mV_{PP}
		R_L = 10kΩ, C_L = 10pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	35 145 190			
—	Crosstalk Between Any Two Switches (Figure 12) (Test does not apply to VHC4051)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600Ω, C_L = 50pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	–50 –50 –50			dB
		f_{in} = 1.0MHz, R_L = 50Ω, C_L = 10pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	–60 –60 –60			
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1kHz, R_L = 10kΩ, C_L = 50pF $THD = THD_{measured} - THD_{source}$ V_{IS} = 4.0V_{PP} sine wave V_{IS} = 8.0V_{PP} sine wave V_{IS} = 11.0V_{PP} sine wave	 2.25 4.50 6.00	 –2.25 –4.50 –6.00	 0.10 0.08 0.05			%

*Limits not tested. Determined by design and verified by qualification.

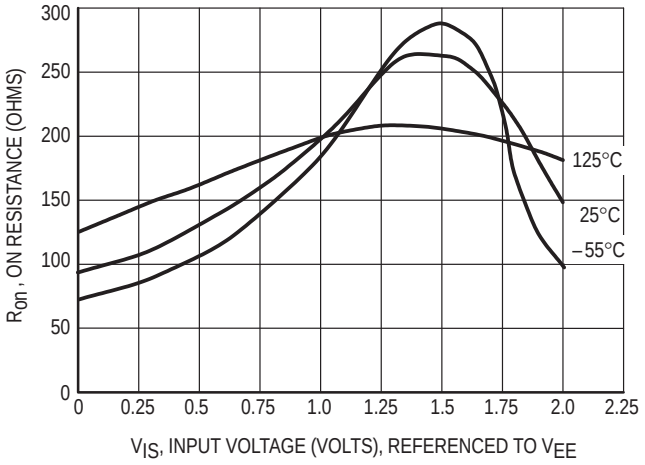


Figure 1a. Typical On Resistance, $V_{CC} - V_{EE}$ = 2.0 V

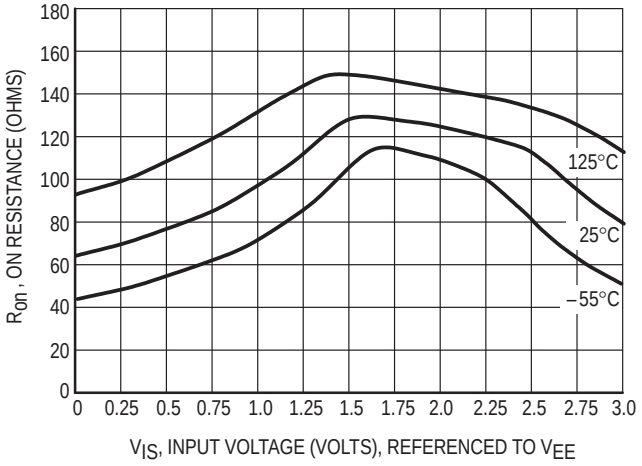


Figure 1b. Typical On Resistance, $V_{CC} - V_{EE}$ = 3.0 V

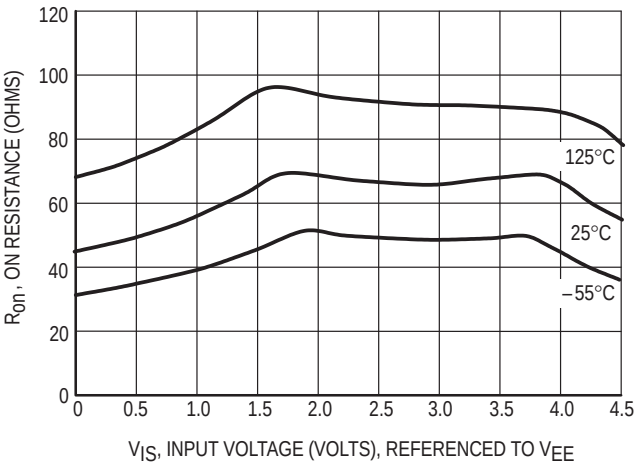


Figure 1c. Typical On Resistance, $V_{CC} - V_{EE}$ = 4.5 V

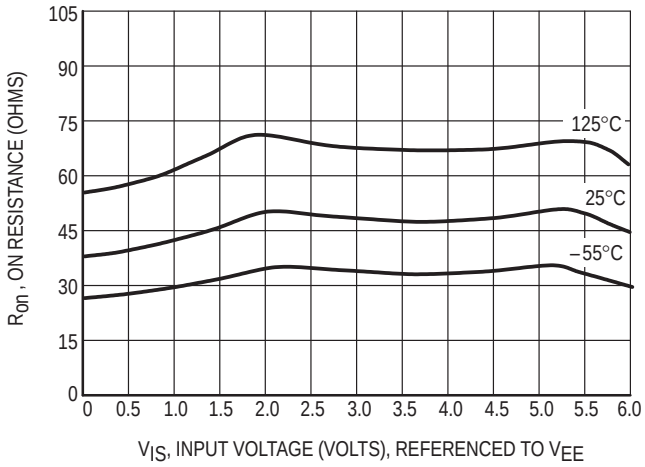


Figure 1d. Typical On Resistance, $V_{CC} - V_{EE}$ = 6.0 V

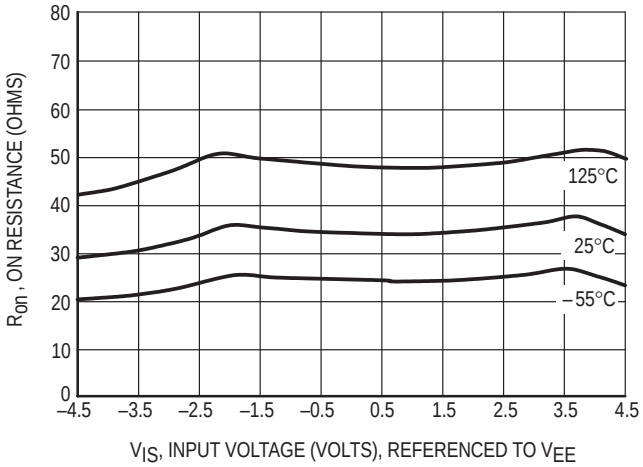


Figure 1e. Typical On Resistance, $V_{CC} - V_{EE}$ = 9.0 V

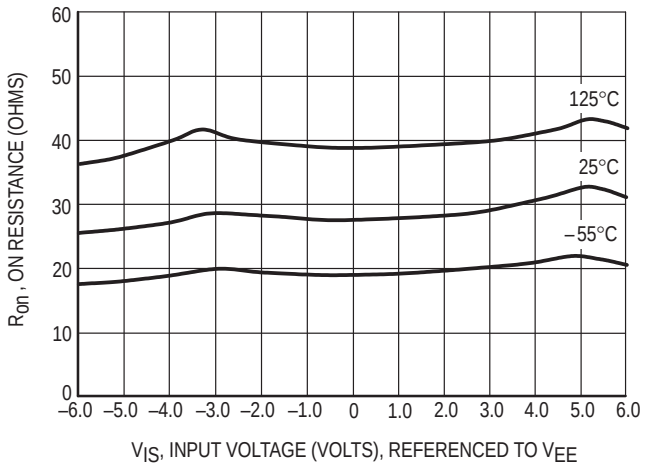


Figure 1f. Typical On Resistance, $V_{CC} - V_{EE}$ = 12.0 V

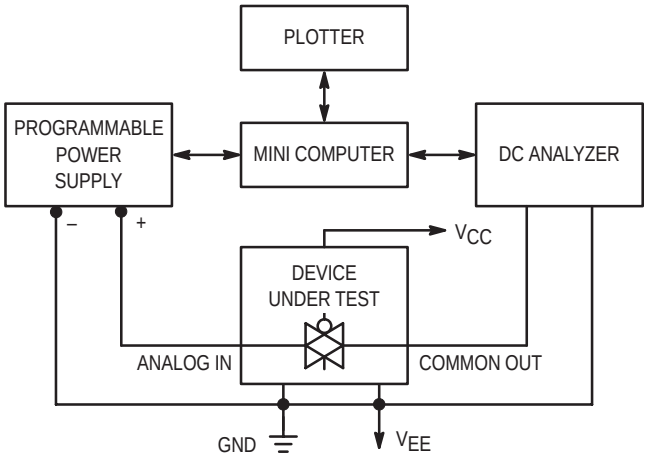


Figure 1. On Resistance Test Set–Up

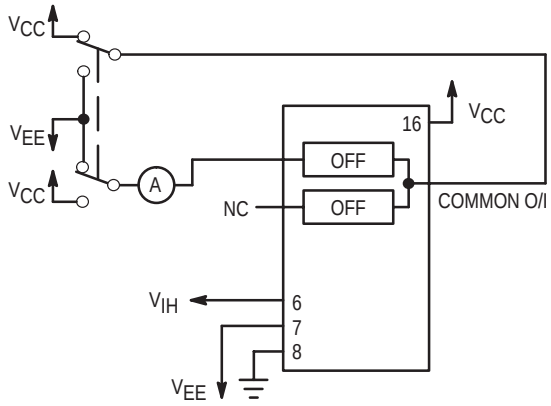


Figure 2. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

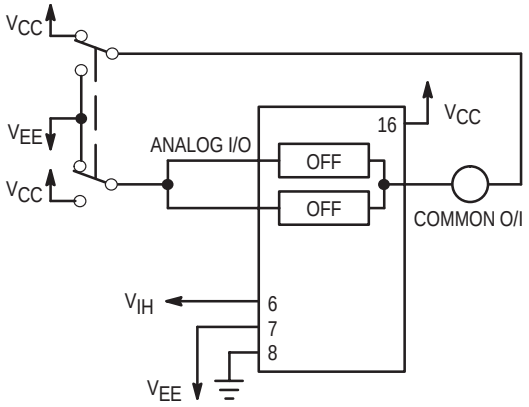


Figure 3. Maximum Off Channel Leakage Current, Common Channel, Test Set–Up

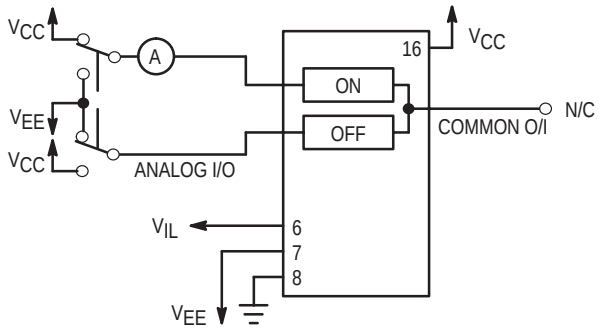


Figure 4. Maximum On Channel Leakage Current, Channel to Channel, Test Set–Up

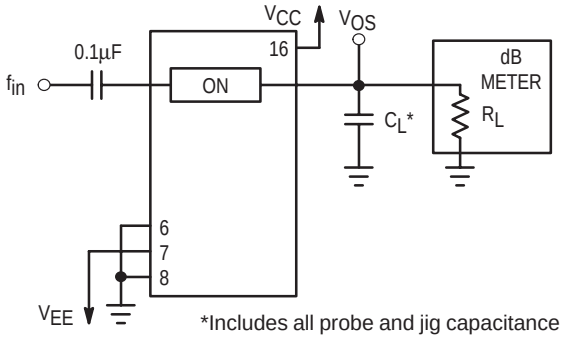


Figure 5. Maximum On Channel Bandwidth, Test Set–Up

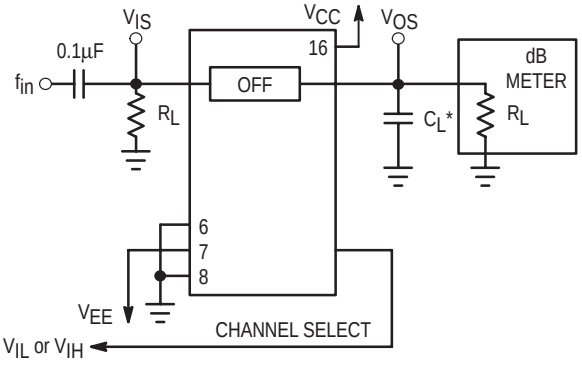


Figure 6. Off Channel Feedthrough Isolation, Test Set–Up

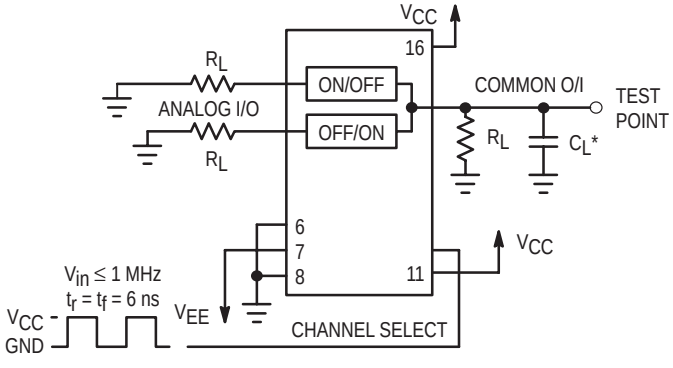


Figure 7. Feedthrough Noise, Channel Select to Common Out, Test Set–Up

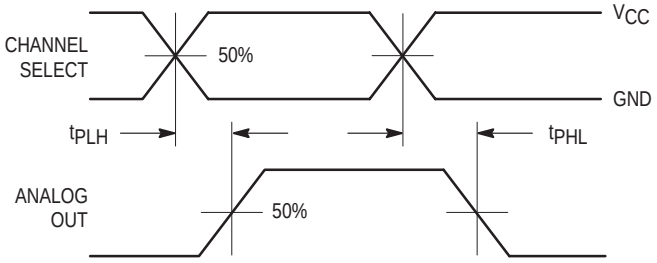
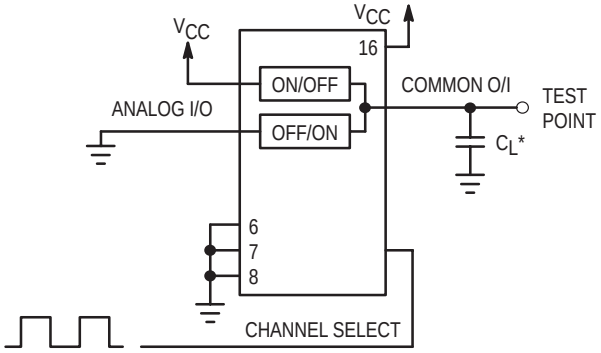


Figure 9a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 8b. Propagation Delay, Test Set–Up Channel Select to Analog Out

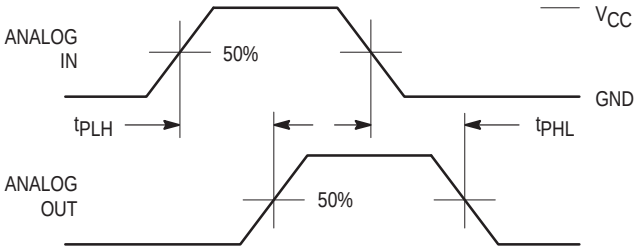
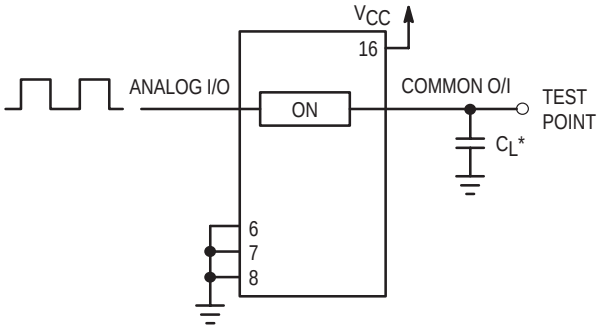


Figure 10a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 9b. Propagation Delay, Test Set–Up Analog In to Analog Out

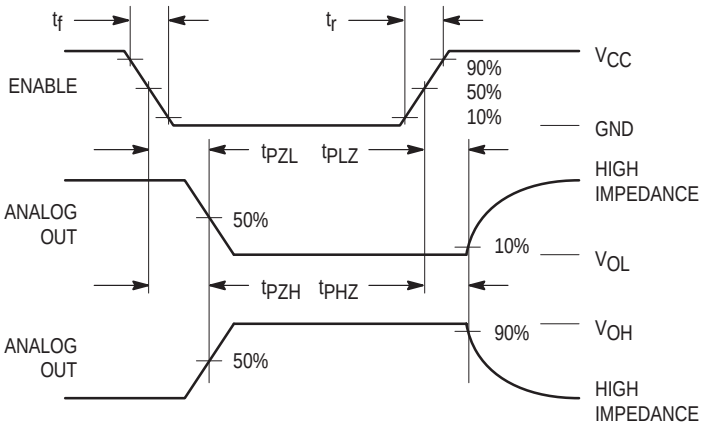


Figure 11a. Propagation Delays, Enable to Analog Out

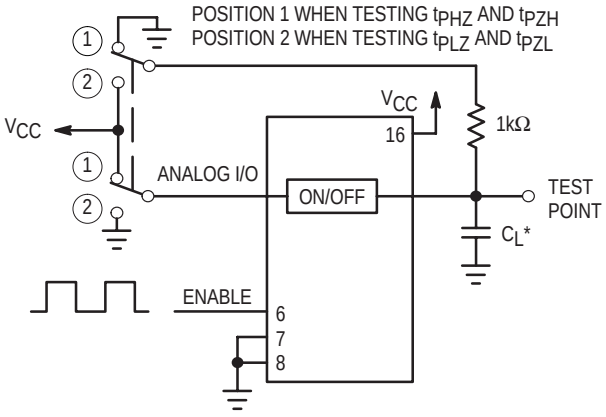


Figure 10b. Propagation Delay, Test Set–Up Enable to Analog Out

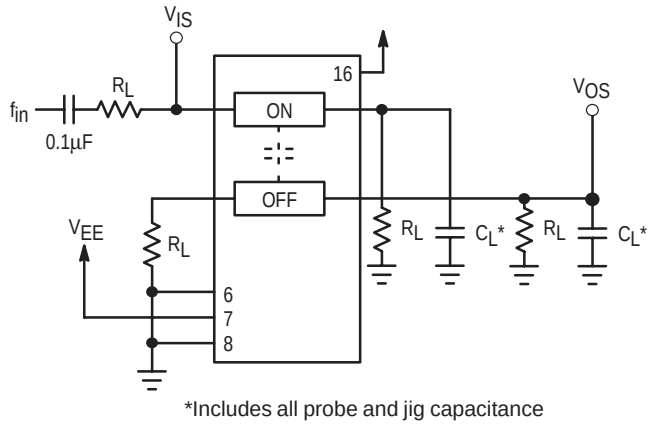


Figure 11. Crosstalk Between Any Two Switches, Test Set–Up

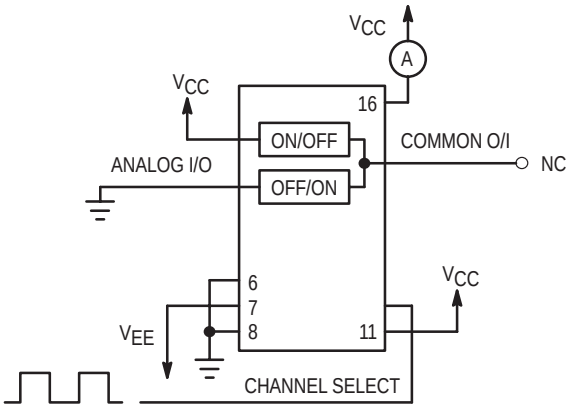


Figure 12. Power Dissipation Capacitance, Test Set–Up

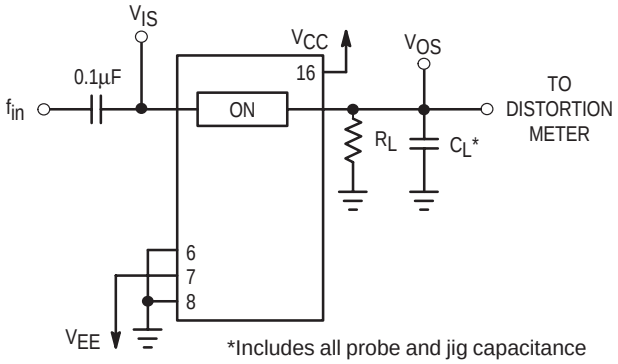


Figure 14a. Total Harmonic Distortion, Test Set–Up

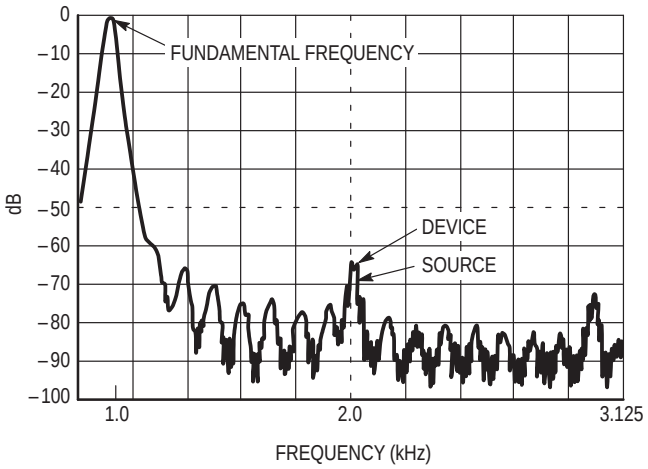


Figure 13b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

V_{CC} = +5V = logic high
GND = 0V = logic low

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below V_{EE}. In this example, the difference between V_{CC} and V_{EE} is ten volts. Therefore, using the configuration of Figure 15, a maximum analog signal of ten volts peak–to–peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

V_{CC} – GND = 2 to 6 volts
V_{EE} – GND = 0 to –6 volts
V_{CC} – V_{EE} = 2 to 12 volts
and $V_{EE} \leq$ GND

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external Germanium or Schottky diodes (D_X) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

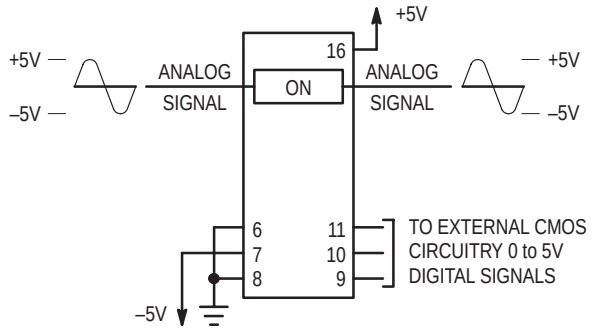


Figure 14. Application Example

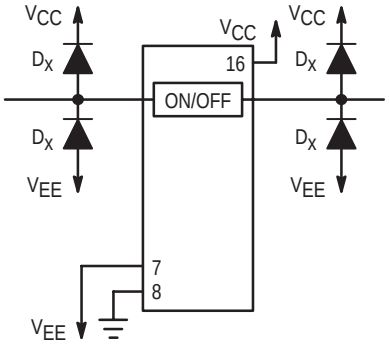
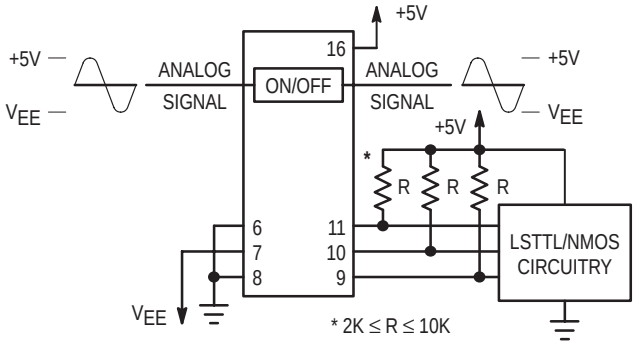
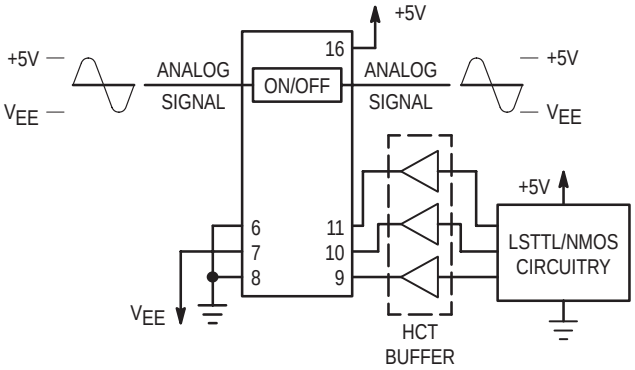


Figure 15. External Germanium or Schottky Clipping Diodes



a. Using Pull–Up Resistors



b. Using HCT Interface

Figure 16. Interfacing LSTTL/NMOS to CMOS Inputs

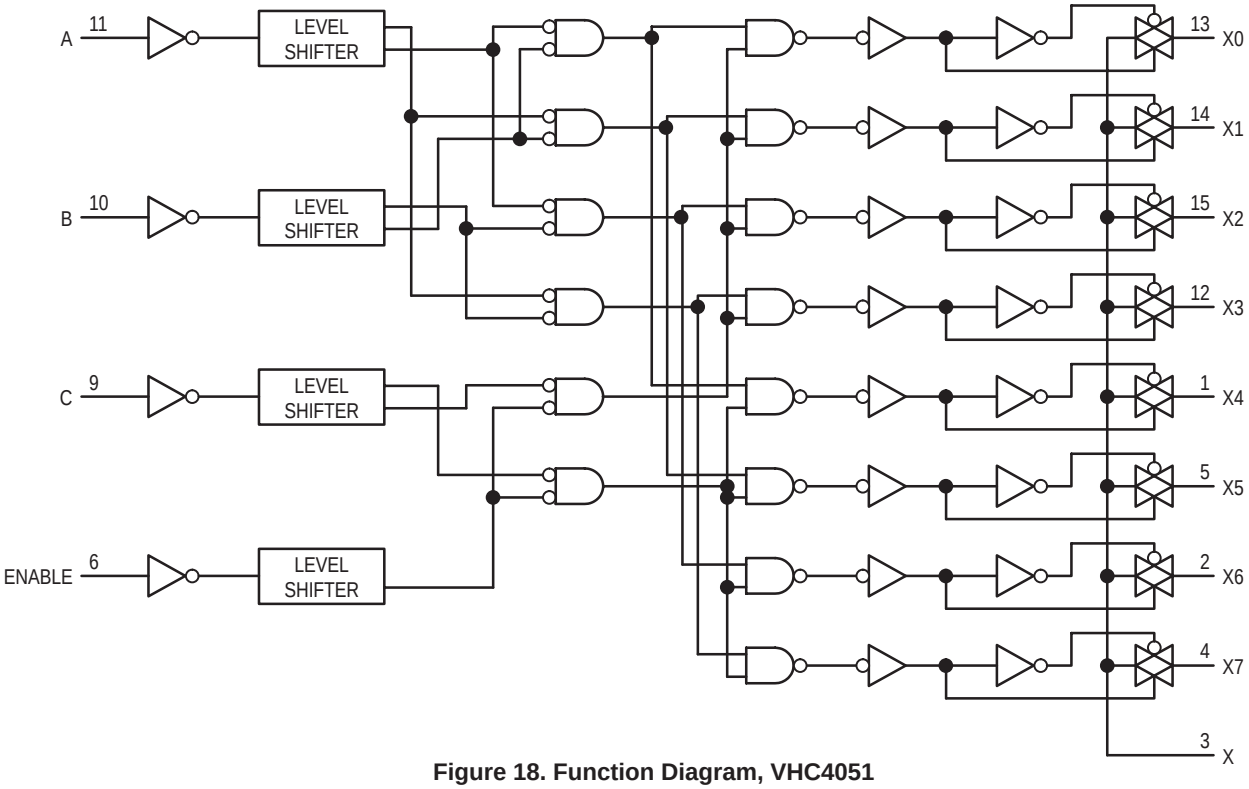


Figure 18. Function Diagram, VHC4051

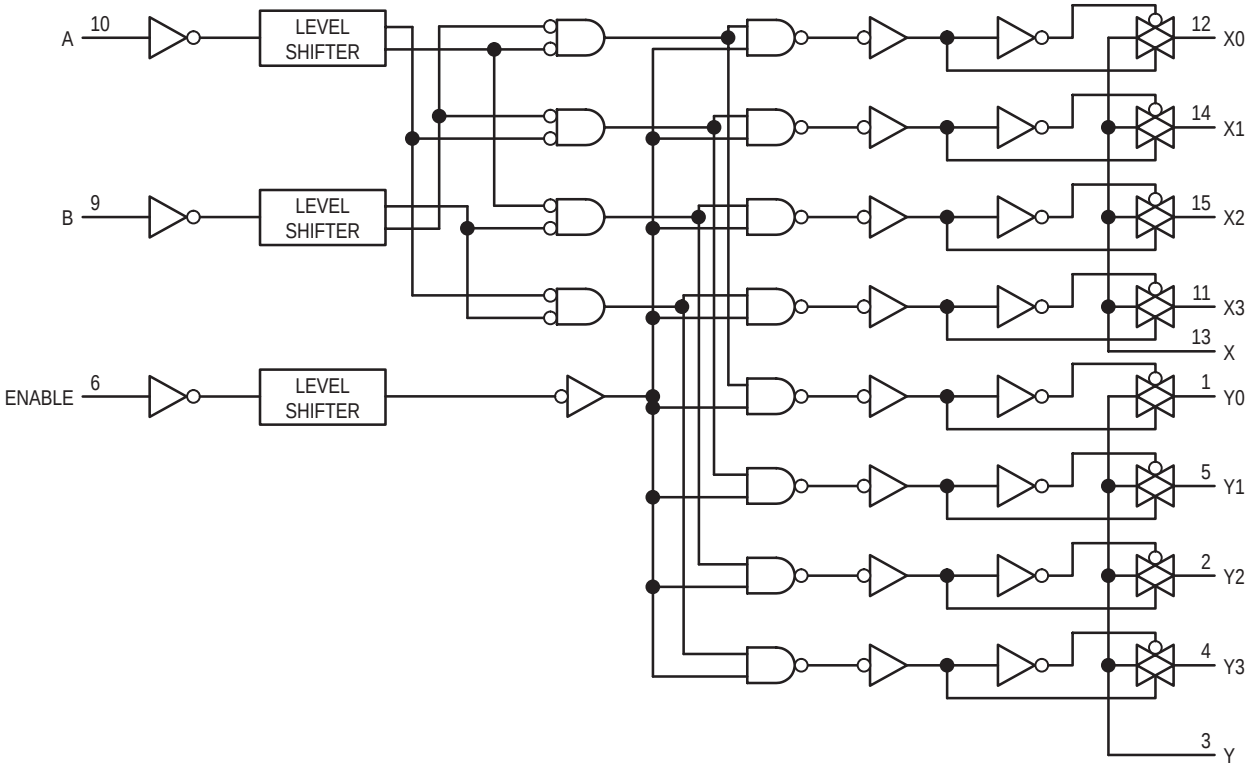


Figure 19. Function Diagram, VHC4052

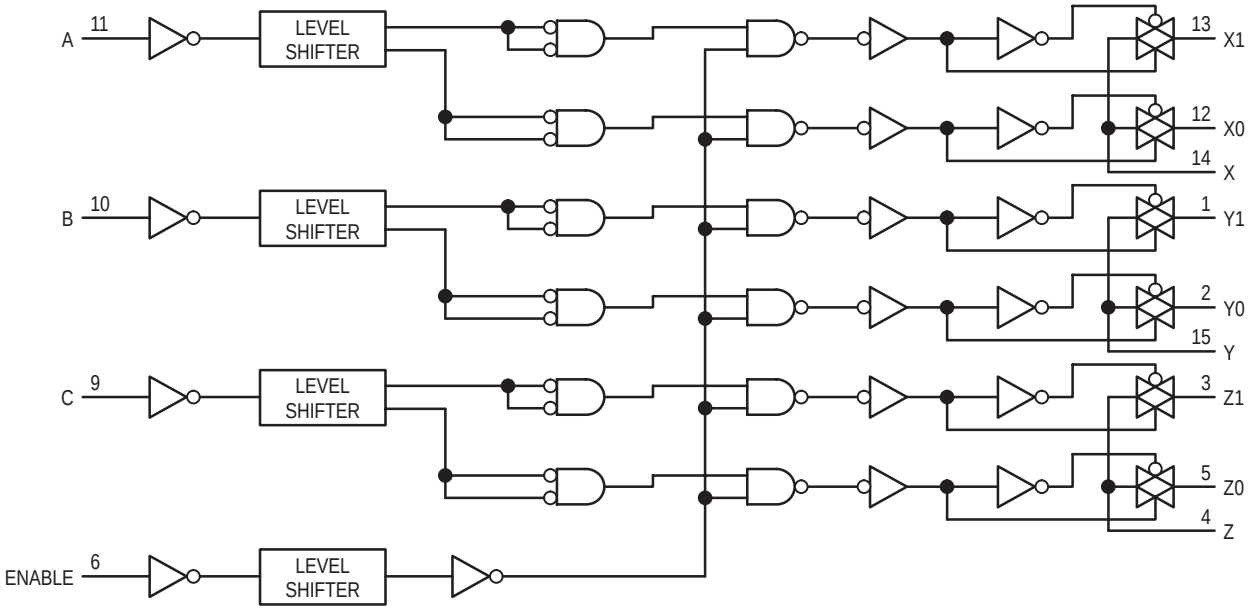


Figure 20. Function Diagram, VHC4053

ORDERING & SHIPPING INFORMATION

Device	Package	Shipping
MC74VHC4051D	SOIC–16	48 Units / Rail
MC74VHC4051DR2	SOIC–16	2500 Units / Tape & Reel
MC74VHC4051DT	TSSOP–16	96 Units / Rail
MC74VHC4051DTR2	TSSOP–16	2500 Units / Tape & Reel
MC74VHC4052D	SOIC–16	48 Units / Rail
MC74VHC4052DR2	SOIC–16	2500 Units / Tape & Reel
MC74VHC4052DT	TSSOP–16	96 Units / Rail
MC74VHC4052DTR2	TSSOP–16	2500 Units / Tape & Reel
MC74VHC4053D	SOIC–16	48 Units / Rail
MC74VHC4053DR2	SOIC–16	2500 Units / Tape & Reel
MC74VHC4053DT	TSSOP–16	96 Units / Rail
MC74VHC4053DTR2	TSSOP–16	2500 Units / Tape & Reel

MC74VHC1G66

Advance Information

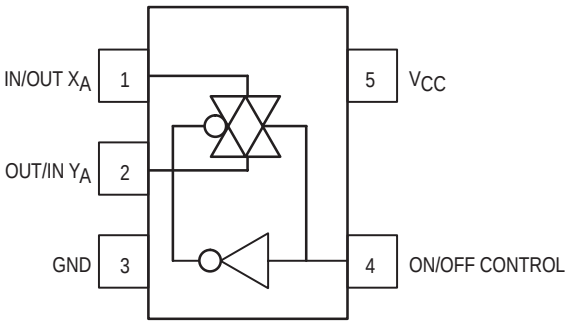
Analog Switch

The MC74VHC1G66 is an advanced high speed CMOS bilateral analog switch fabricated with silicon gate CMOS technology. It achieves high speed propagation delays and low ON resistances while maintaining CMOS low power dissipation. This bilateral switch controls analog and digital voltages that may vary across the full power–supply range (from V_{CC} to GND).

The MC74VHC1G66 is compatible in function to a single gate of the High Speed CMOS MC74VHC4066 and the metal–gate CMOS MC14066. The device has been designed so that the ON resistances (R_{ON}) are much lower and more linear over input voltage than R_{ON} of the metal–gate CMOS or High Speed CMOS analog switches.

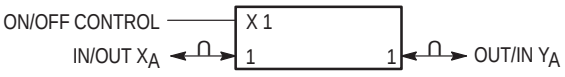
The ON/OFF control inputs are compatible with standard CMOS outputs; with pull–up resistors, it is compatible with LSTTL outputs.

- High Speed: t_{PD} = **TBD** (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- Diode Protection Provided on Inputs and Outputs
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14066 or the HC4066
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; MM > 200 V, CDM > 1500 V
- Chip Complexity: 11 FETs or 3 Equivalent Gates



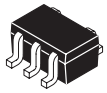
5–Lead SOT–353 Pinout (Top View)

LOGIC SYMBOL



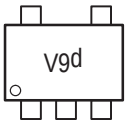
ON Semiconductor

http://onsemi.com



SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	IN/OUT X_A
2	OUT/IN Y_A
3	GND
4	ON/OFF CONTROL
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 117 of this data sheet.

FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	–0.5 to +7.0	V
Digital Input Voltage	V_{IN}	–0.5 to V_{CC} +0.5	V
Analog Output Voltage	V_{IS}	–0.5 to V_{CC} + 0.5	V
Digital Input Diode Current	I_{IK}	–20	mA
DC Supply Current, V_{CC} and GND	I_{CC}	+25	mA
Power dissipation in still air, SC–88A †	P_D	200	mW
Lead temperature, 1 mm from case for 10 s	T_L	260	°C
Storage temperature	T_{stg}	–65 to +150	°C

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	4.5	5.5	V
Digital Input Voltage		V_{IN}	GND	V_{CC}	V
Analog Input Voltage		V_{IS}	GND	V_{CC}	V
Static or Dynamic Voltage Across Switch		V_{IO}*		1.2	V
Operating Temperature Range		T_A	–55	+85	°C
Input Rise and Fall Time		t_r , t_f			ns/V
ON/OFF Control Input	V_{CC} = 3.3V ± 0.3V		0	100	
	V_{CC} = 5.0V ± 0.5V		0	20	

* For voltage drops across the switch greater than 1.2V (switch on), excessive V_{CC} current may be drawn; i.e. the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			$T_A \le 85°C$		$T_A \le 125°C$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage ON/OFF Control Input	R_{ON} = Per Spec	2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low–Level Input Voltage ON/OFF Control Input	R_{ON} = Per Spec	2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
I_{IN}	Maximum Input Leakage Current ON/OFF Control Input	V_{IN} = V_{CC} or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND V_{IO} = 0V	5.5			2.0		20		40	μA
R_{ON}	Maximum "ON" Resistance	V_{IN} = V_{IH} V_{IS} = V_{CC} or GND $\|I_{IS}\| \le$ 10mA (Figure 1)	3.0 4.5 5.5		30 20 15	50 30 20		70 40 35		100 50 45	Ω
		Endpoints V_{IN} = V_{IH} V_{IS} = V_{CC} or GND $\|I_{IS}\| \le$ 10mA (Figure 1)	3.0 4.5 5.5		25 12 8	50 20 15		65 26 23		90 40 32	Ω
I_{OFF}	Maximum Off–Channel Leakage Current	V_{IN} = V_{IL} V_{IS} = V_{CC} or GND Switch Off (Figure 2)	5.5			0.1		0.5		1.0	μA
I_{ON}	Maximum On–Channel Leakage Current	V_{IN} = V_{IH} V_{IS} = V_{CC} or GND Switch On (Figure 3)	5.5			0.1		0.5		1.0	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input t_r/t_f = 3.0ns)

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			$T_A \le 85°C$		$T_A \le 125°C$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input X to Y	Y_A = Open Figure 4	2.0 3.0 4.5 5.5		1 0 0 0	5 2 1 1		6 3 1 1		7 4 2 1	ns
t_{PLZ}, t_{PHZ}	Maximum Propogation Delay, ON/OFF Control to Analog Output	R_L = 1000 Ω Figure 5	2.0 3.0 4.5 5.5		15 8 6 4	35 15 10 7		46 20 13 9		57 25 17 11	ns
t_{PZL}, t_{PZH}	Maximum Propogation Delay, ON/OFF Control to Analog Output	R_L = 1000 Ω Figure 5	2.0 3.0 4.5 5.5		15 8 6 4	35 15 10 7		46 20 13 9		57 25 17 11	ns
C_{IN}	Maximum Input Capacitance	ON/OFF Control Input	0.0		3	10		10		10	pF
		Contol Input = GND Analog I/O Feedthrough	5.0		 4 4	 10 10		 10 10		 10 10	

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note NO TAG)	18	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Test Conditions	V_{CC}	Limit 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response Figure 7	f_{in} = 1 MHz Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{OS} Increase f_{in} = frequency until dB meter reads –3dB R_L = 50Ω, C_L = 10 pF	3.0 4.5 5.5	150 175 200	MHz
ISO_{off}	Off–Channel Feedthrough Isolation Figure 8	f_{in} = Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600Ω, C_L = 50 pF	3.0 4.5 5.5	–50 –50 –50	dB
		f_{in} = 1.0 kHz, R_L = 50Ω, C_L = 10 pF	3.0 4.5 5.5	–40 –40 –40	
$NOISE_{feed}$	Feedthrough Noise Control to Switch Figure 9	V_{in} ≤ 1 MHz Square Wave (t_r = t_f = 2ns) Adjust R_L at setup so that I_S = 0 A R_L = 600Ω, C_L = 50 pF	3.0 4.5 5.5	45 60 130	mV_{PP}
		R_L = 50Ω, C_L = 10 pF	3.0 4.5 5.5	25 30 60	
THD	Total Harmonic Distortion Figure 10	f_{in} = 1 kHz, R_L = 10kΩ, C_L = 50 pF $THD = THD_{Measured} - THD_{Source}$ V_{IS} = 3.0 V_{PP} sine wave V_{IS} = 4.0 V_{PP} sine wave V_{IS} = 5.0 V_{PP} sine wave	 3.3 4.5 5.5	 0.20 0.10 0.06	%

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

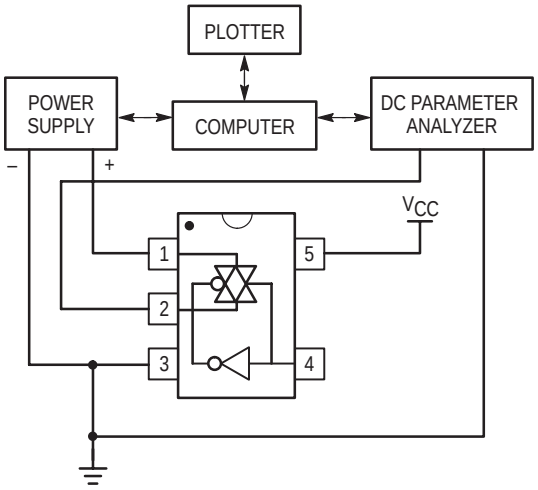


Figure 1. On Resistance Test Set–Up

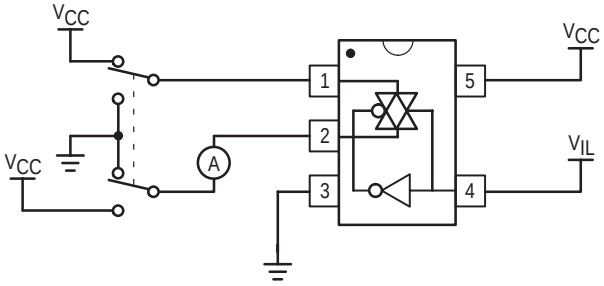


Figure 2. Maximum Off–Channel Leakage Current Test Set–Up

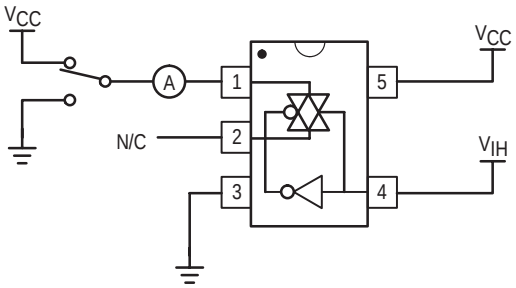


Figure 3. Maximum On–Channel Leakage Current Test Set–Up

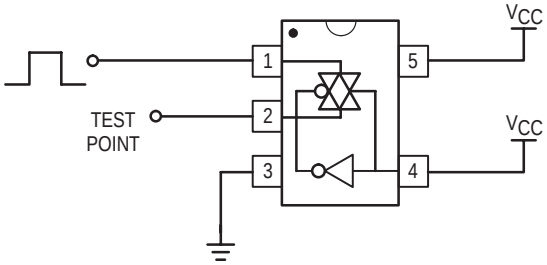


Figure 4. Propagation Delay Test Set–Up

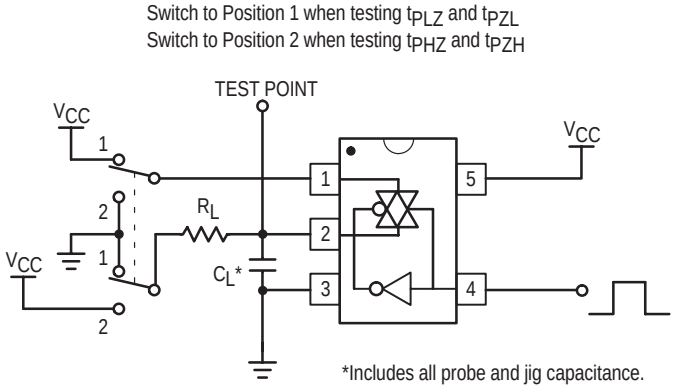


Figure 5. Propagation Delay Output Enable/Disable Test Set–Up

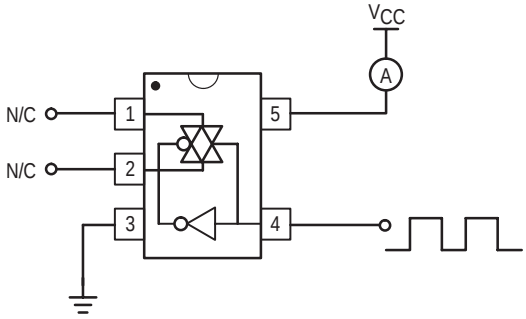


Figure 6. Power Dissipation Capacitance Test Set–Up

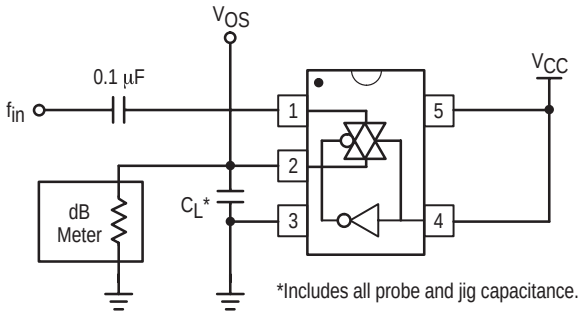


Figure 7. Maximum On–Channel Bandwidth Test Set–Up

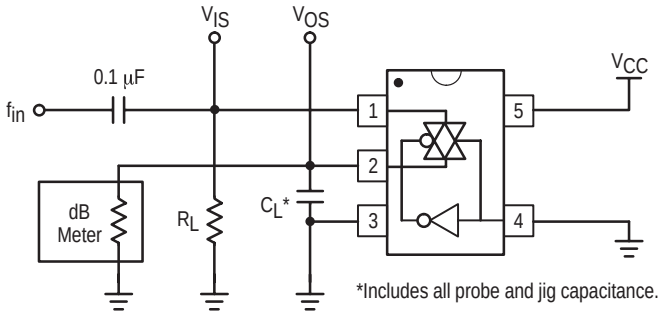


Figure 8. Off–Channel Feedthrough Isolation Test Set–Up

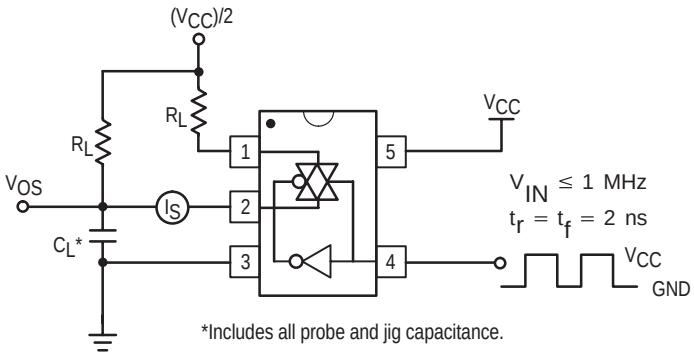


Figure 9. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set–Up

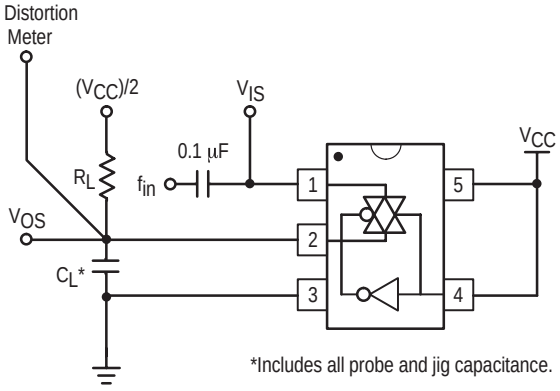


Figure 10. Total Harmonic Distortion Test Set–Up

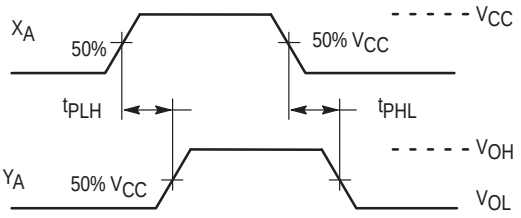


Figure 11. Propagation Delay, Analog In to Analog Out Waveforms

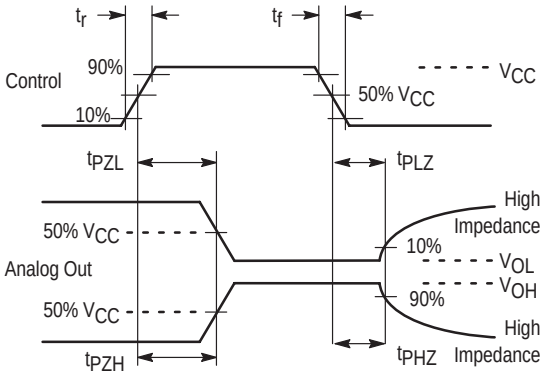


Figure 12. Propagation Delay, ON/OFF Control

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1G66DFT1	MC	74	VHC1G	66	DF	T1	SC–88A / SOT–353	7–Inch/3000 Unit

MC74VHC1GT66

Advance Information

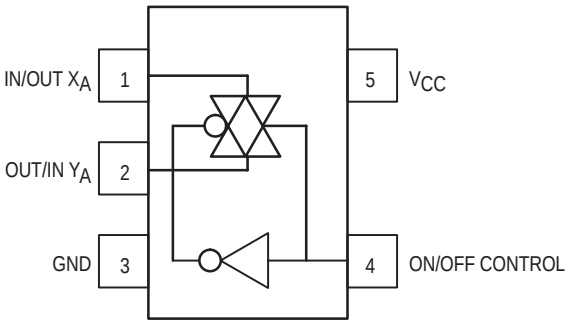
Analog Switch

The MC74VHC1GT66 is an advanced high speed CMOS bilateral analog switch fabricated with silicon gate CMOS technology. It achieves high speed propagation delays and low ON resistances while maintaining CMOS low power dissipation. This bilateral switch controls analog and digital voltages that may vary across the full power–supply range (from V_{CC} to GND).

The MC74VHC1GT66 is compatible in function to a single gate of the very High Speed CMOS MC74VHCT4066. The device has been designed so that the ON resistances (R_{ON}) are much lower and more linear over input voltage than R_{ON} of the metal–gate CMOS or High Speed CMOS analog switches.

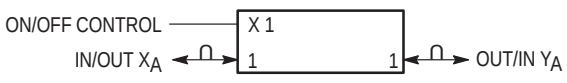
The ON/OFF Control input is compatible with TTL–type input thresholds allowing the device to be used as a logic–level translator from 3.0V CMOS logic to 5.0V CMOS logic or from 1.8V CMOS logic to 3.0V CMOS logic while operating at the high–voltage power supply. The input protection circuitry on this device allows overvoltage tolerance on the input, which provides protection when voltages of up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1GT66 to be used to interface 5V circuits to 3V circuits.

- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- Diode Protection Provided on Inputs and Outputs
- Improved Linearity and Lower ON Resistance over Input Voltage
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; MM > 200 V, CDM > 1500 V



5–Lead SOT–353 Pinout (Top View)

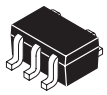
LOGIC SYMBOL



This document contains information on a new product. Specifications and information herein are subject to change without notice.

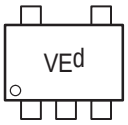
ON Semiconductor

http://onsemi.com



SC–88A / SOT–353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	IN/OUT X_A
2	OUT/IN Y_A
3	GND
4	ON/OFF CONTROL
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 124 of this data sheet.

FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	–0.5 to +7.0	V
Digital Input Voltage	V_{IN}	–0.5 to V_{CC} +0.5	V
Analog Output Voltage	V_{IS}	–0.5 to V_{CC} + 0.5	V
Digital Input Diode Current	I_{IK}	–20	mA
DC Supply Current, V_{CC} and GND	I_{CC}	+25	mA
Power dissipation in still air, SC–88A †	P_D	200	mW
Lead temperature, 1 mm from case for 10 s	T_L	260	°C
Storage temperature	T_{stg}	–65 to +150	°C

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	4.5	5.5	V
Digital Input Voltage		V_{IN}	GND	V_{CC}	V
Analog Input Voltage		V_{IS}	GND	V_{CC}	V
Static or Dynamic Voltage Across Switch		V_{IO}*		1.2	V
Operating Temperature Range		T_A	–55	+85	°C
Input Rise and Fall Time		t_r , t_f			ns/V
ON/OFF Control Input	V_{CC} = 3.3V ± 0.3V		0	100	
	V_{CC} = 5.0V ± 0.5V		0	20	

* For voltage drops across the switch greater than 1.2V (switch on), excessive V_{CC} current may be drawn; i.e. the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			$T_A \le 85°C$		$T_A \le 125°C$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage ON/OFF Control Input	R_{ON} = Per Spec	3.0 4.5 5.5	1.2 2.0 2.0			1.2 2.0 2.0		1.2 2.0 2.0		V
V_{IL}	Maximum Low–Level Input Voltage ON/OFF Control Input	R_{ON} = Per Spec	3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
I_{IN}	Maximum Input Leakage Current ON/OFF Control Input	V_{IN} = V_{CC} or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND V_{IO} = 0V	5.5			2.0		20		40	μA
I_{CCT}	Quiescent Supply Current	ON/OFF Control at 3.4V	5.5			1.35		1.5		1.65	mA
R_{ON}	Maximum "ON" Resistance	V_{IN} = V_{IH} V_{IS} = V_{CC} or GND $\|I_{IS}\| \le$ 10mA (Figure 1)	3.0 4.5 5.5		30 20 15	50 30 20		70 40 35		100 50 45	Ω
		Endpoints V_{IN} = V_{IH} V_{IS} = V_{CC} or GND $\|I_{IS}\| \le$ 10mA (Figure 1)	3.0 4.5 5.5		25 12 8	50 20 15		65 26 23		90 40 32	Ω
I_{OFF}	Maximum Off–Channel Leakage Current	V_{IN} = V_{IL} V_{IS} = V_{CC} or GND Switch Off (Figure 2)	5.5			0.1		0.5		1.0	μA
I_{ON}	Maximum On–Channel Leakage Current	V_{IN} = V_{IH} V_{IS} = V_{CC} or GND Switch On (Figure 3)	5.5			0.1		0.5		1.0	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input t_r/t_f = 3.0ns)

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			$T_A \le 85°C$		$T_A \le 125°C$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input X to Y	Y_A = Open Figure 4	2.0 3.0 4.5 5.5		1 0 0 0	5 2 1 1		6 3 1 1		7 4 2 1	ns
t_{PLZ}, t_{PHZ}	Maximum Propogation Delay, ON/OFF Control to Analog Output	R_L = 1000 Ω Figure 5	2.0 3.0 4.5 5.5		15 8 6 4	35 15 10 7		46 20 13 9		57 25 17 11	ns
t_{PZL}, t_{PZH}	Maximum Propogation Delay, ON/OFF Control to Analog Output	R_L = 1000 Ω Figure 5	2.0 3.0 4.5 5.5		15 8 6 4	35 15 10 7		46 20 13 9		57 25 17 11	ns
C_{IN}	Maximum Input Capacitance	ON/OFF Control Input	0.0		3	10		10		10	pF
		Contol Input = GND Analog I/O Feedthrough	5.0		 4 4	 10 10		 10 10		 10 10	

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note NO TAG)	18	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Test Conditions	V_{CC}	Limit 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response Figure 7	f_{in} = 1 MHz Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{OS} Increase f_{in} = frequency until dB meter reads –3dB R_L = 50Ω, C_L = 10 pF	3.0 4.5 5.5	150 175 200	MHz
ISO_{off}	Off–Channel Feedthrough Isolation Figure 8	f_{in} = Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600Ω, C_L = 50 pF	3.0 4.5 5.5	–50 –50 –50	dB
		f_{in} = 1.0 kHz, R_L = 50Ω, C_L = 10 pF	3.0 4.5 5.5	–40 –40 –40	
$NOISE_{feed}$	Feedthrough Noise Control to Switch Figure 9	V_{in} ≤ 1 MHz Square Wave (t_r = t_f = 2ns) Adjust R_L at setup so that I_S = 0 A R_L = 600Ω, C_L = 50 pF	3.0 4.5 5.5	45 60 130	mV_{PP}
		R_L = 50Ω, C_L = 10 pF	3.0 4.5 5.5	25 30 60	
THD	Total Harmonic Distortion Figure 10	f_{in} = 1 kHz, R_L = 10kΩ, C_L = 50 pF $THD = THD_{Measured} - THD_{Source}$ V_{IS} = 3.0 V_{PP} sine wave V_{IS} = 4.0 V_{PP} sine wave V_{IS} = 5.0 V_{PP} sine wave	 3.3 4.5 5.5	 0.20 0.10 0.06	%

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

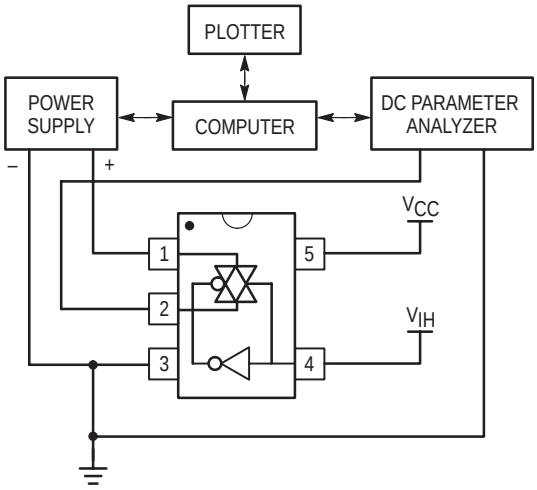


Figure 1. On Resistance Test Set–Up

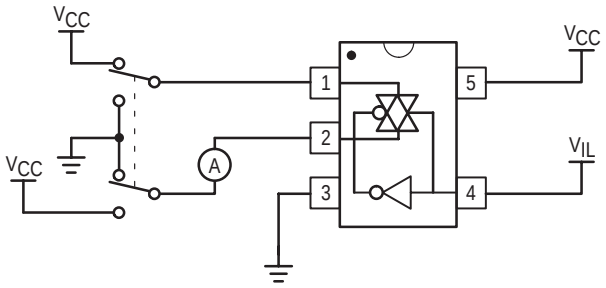


Figure 2. Maximum Off–Channel Leakage Current Test Set–Up

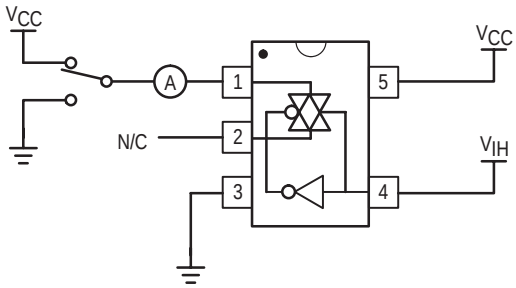


Figure 3. Maximum On–Channel Leakage Current Test Set–Up

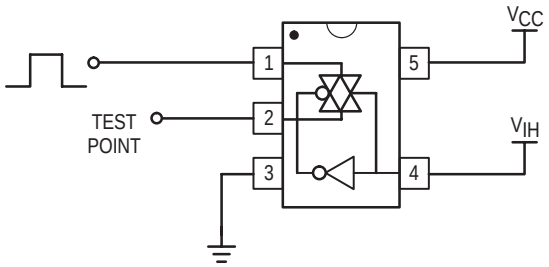


Figure 4. Propagation Delay Test Set–Up

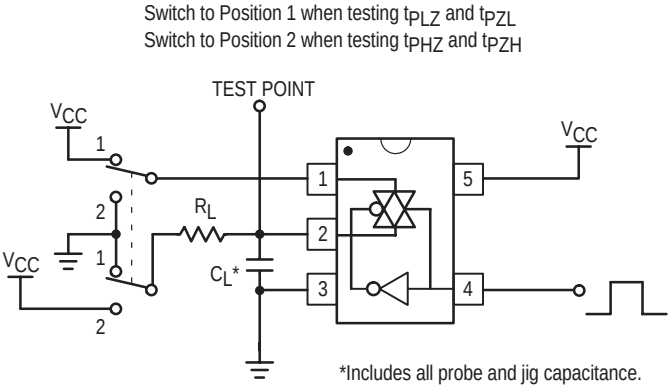


Figure 5. Propagation Delay Output Enable/Disable Test Set–Up

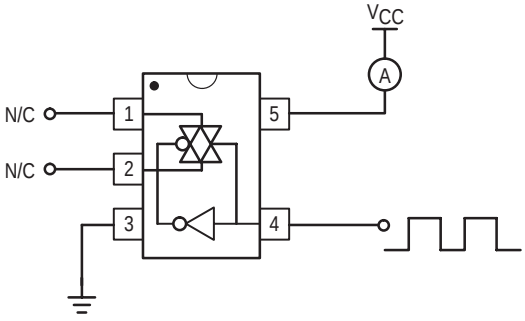


Figure 6. Power Dissipation Capacitance Test Set–Up

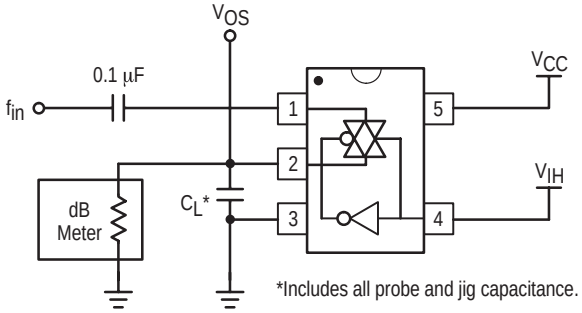


Figure 7. Maximum On–Channel Bandwidth Test Set–Up

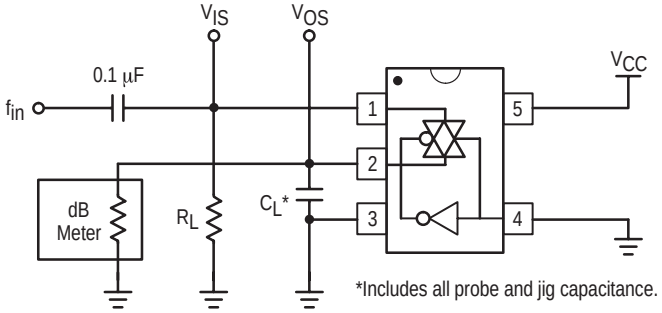


Figure 8. Off–Channel Feedthrough Isolation Test Set–Up

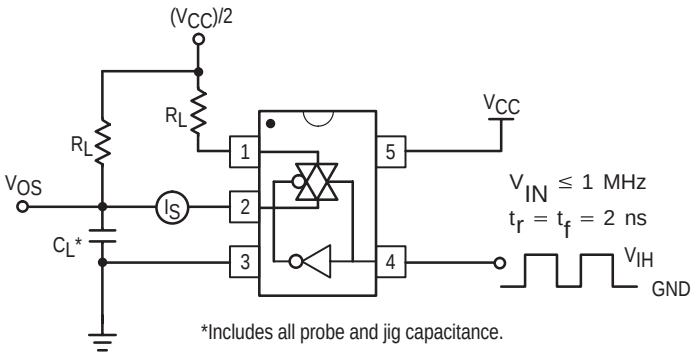


Figure 9. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set–Up

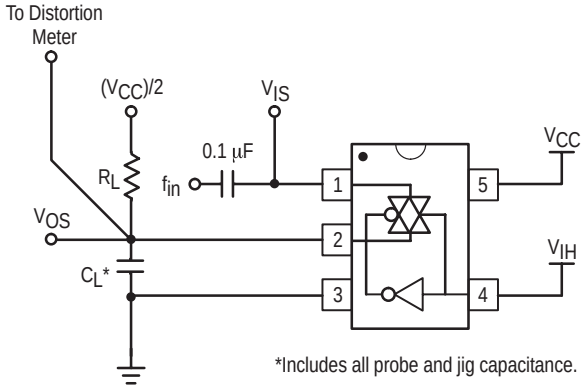


Figure 10. Total Harmonic Distortion Test Set–Up

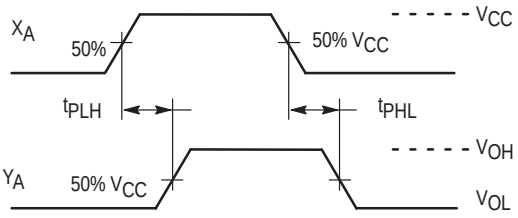


Figure 11. Propagation Delay, Analog In to Analog Out Waveforms

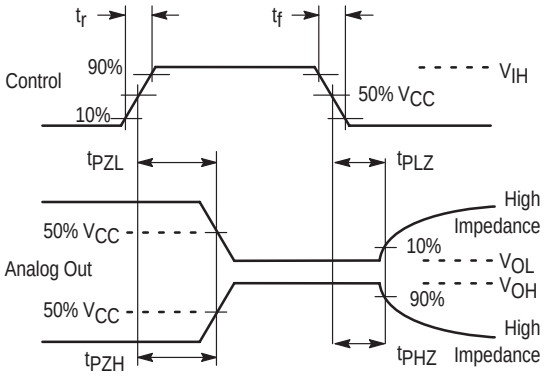


Figure 12. Propagation Delay, ON/OFF Control

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1GT66DFT1	MC	74	VHC1G	T66	DF	T1	SC–88A / SOT–353	7–Inch/3000 Unit

MC74LVX4051

Product Preview

Analog Multiplexer / Demultiplexer

High–Performance Silicon–Gate CMOS

The MC74LVX4051 utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

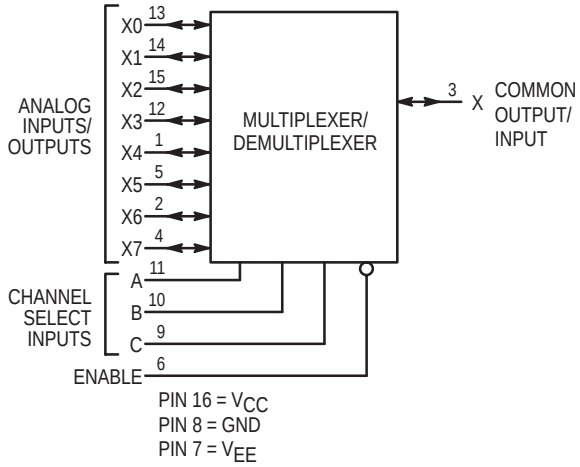
The LVX4051 is similar in pinout to the LVX8051, HC4051A and the metal–gate MC14051B. The Channel–Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel–Select and Enable inputs are compatible with standard CMOS outputs; with pull–up resistors they are compatible with LSTTL outputs.

This device has been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal–gate CMOS analog switches.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Digital (Control) Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal–Gate Counterparts
- Low Noise

LOGIC DIAGRAM
MC74LVX4051
Single–Pole, 8–Position Plus Common Off



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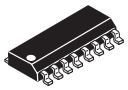
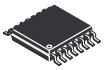
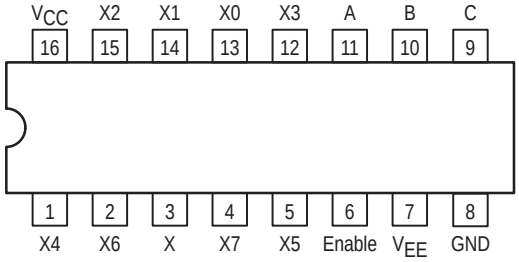


16–LEAD SOIC
D SUFFIX
CASE 751B



16–LEAD TSSOP
DT SUFFIX
CASE 948F

PIN CONNECTION AND MARKING DIAGRAM (Top View)



ORDERING INFORMATION

Device	Package	Shipping
MC74LVX4051D	SOIC	TBD
MC74LVX4051DT	TSSOP	TBD

FUNCTION TABLE – MC74LVX4051

Control Inputs				
	Select			
Enable	C	B	A	ON Channels
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

X = Don't Care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	– 7.0 to + 5.0	V
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	– 0.5 to + 7.0 – 0.5 to + 7.0	V
V_{IS}	Analog Input Voltage	– 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin	± 20	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	–6.6	GND	V
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	2.0 2.0	3.3 6.6	V
V_{IS}	Analog Input Voltage	V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)	0	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		1.2	V
T_A	Operating Temperature Range, All Package Types	– 55	+ 85	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs) V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	 0 0	 100 20	ns/V

*For voltage drops across switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

MC74LVX4052

Product Preview

Analog Multiplexer / Demultiplexer

High–Performance Silicon–Gate CMOS

The MC74LVX4052 utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

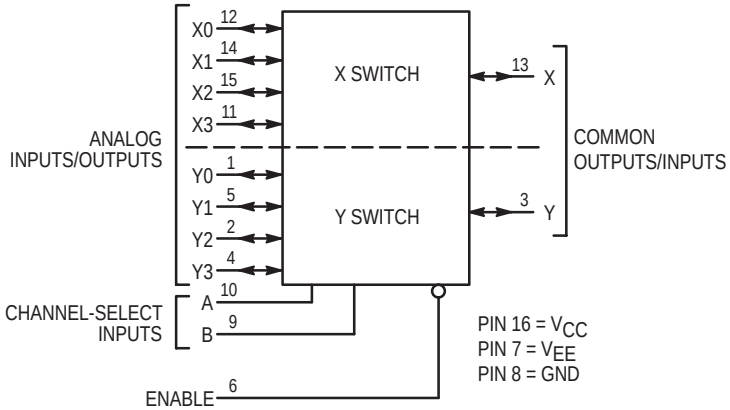
The LVX4052 is similar in pinout to the high–speed HC4052A, and the metal–gate MC14052B. The Channel–Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel–Select and Enable inputs are compatible with standard CMOS outputs; with pull–up resistors they are compatible with LSTTL outputs.

This device has been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal–gate CMOS analog switches.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Digital (Control) Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal–Gate Counterparts
- Low Noise

LOGIC DIAGRAM
MC74LVX4052
Double–Pole, 4–Position Plus Common Off



NOTE: This device allows independent control of each switch. Channel–Select Input A controls the X–Switch, Input B controls the Y–Switch

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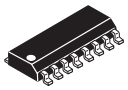
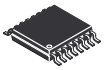
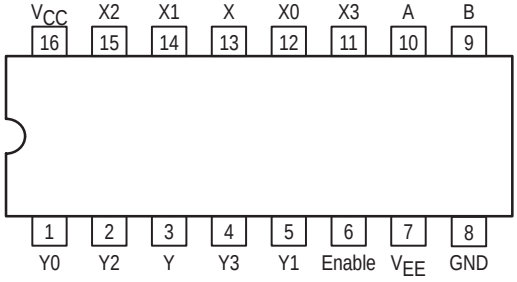


16–LEAD SOIC
D SUFFIX
CASE 751B



16–LEAD TSSOP
DT SUFFIX
CASE 948F

PIN CONNECTION AND MARKING DIAGRAM (Top View)



ORDERING INFORMATION

Device	Package	Shipping
MC74LVX4052D	SOIC	TBD
MC74LVX4052DT	TSSOP	TBD

FUNCTION TABLE – MC74LVX4052

Control Inputs			
Enable	Select B	Select A	ON Channels
L	L	L	Y0 X0
L	L	H	Y1 X1
L	H	L	Y2 X2
L	H	H	Y3 X3
H	X	X	NONE

X = Don't Care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	– 7.0 to + 5.0	V
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	– 0.5 to + 7.0 – 0.5 to + 7.0	V
V_{IS}	Analog Input Voltage	V_{EE} – 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin	± 20	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	–6.6	GND	V
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	2.0 2.0	3.3 6.6	V
V_{IS}	Analog Input Voltage	V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)	0	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		1.2	V
T_A	Operating Temperature Range, All Package Types	– 55	+ 85	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs) V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	 0 0	 100 20	ns/V

*For voltage drops across switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

MC74LVX4053

Product Preview

Analog Multiplexer / Demultiplexer

High–Performance Silicon–Gate CMOS

The MC74LVX4053 utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The LVX4053 is similar in pinout to the LVX8053, HC4053A, and the metal–gate MC14053B. The Channel–Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

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This device has been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal–gate CMOS analog switches.

- Fast Switching and Propagation Speeds
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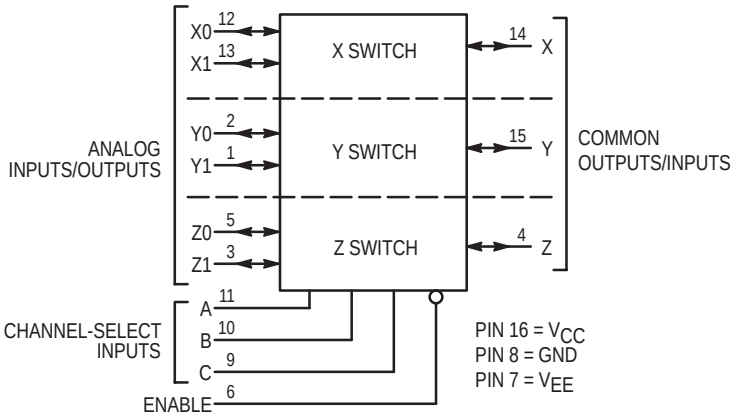
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Digital (Control) Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal–Gate Counterparts
- Low Noise

LOGIC DIAGRAM

Triple Single–Pole, Double–Position Plus Common Off



NOTE: This device allows independent control of each switch. Channel–Select Input A controls the X–Switch, Input B controls the Y–Switch and Input C controls the Z–Switch

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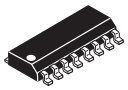
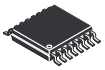
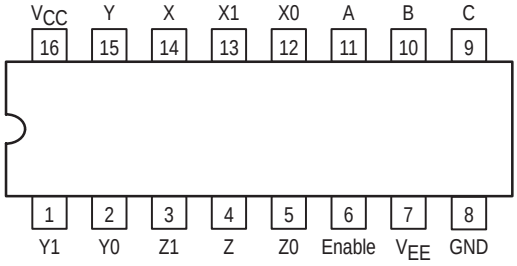


16–LEAD SOIC
D SUFFIX
CASE 751B



16–LEAD TSSOP
DT SUFFIX
CASE 948F

PIN CONNECTION AND MARKING DIAGRAM (Top View)



ORDERING INFORMATION

Device	Package	Shipping
MC74LVX4053D	SOIC	TBD
MC74LVX4053DT	TSSOP	TBD

FUNCTION TABLE – MC74LVX4053

Control Inputs						
	Select			ON Channels		
Enable	C	B	A			
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	NONE		

X = Don't Care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	– 7.0 to + 5.0	V
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	– 0.5 to + 7.0 – 0.5 to + 7.0	V
V_{IS}	Analog Input Voltage	V_{EE} – 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin	± 20	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
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†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
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Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	–6.6	GND	V
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	2.0 2.0	3.3 6.6	V
V_{IS}	Analog Input Voltage	V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)	0	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		1.2	V
T_A	Operating Temperature Range, All Package Types	– 55	+ 85	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs) V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	 0 0	 100 20	ns/V

*For voltage drops across switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

MC74LVX4066

Quad Analog Switch/ Multiplexer/Demultiplexer

High–Performance Silicon–Gate CMOS

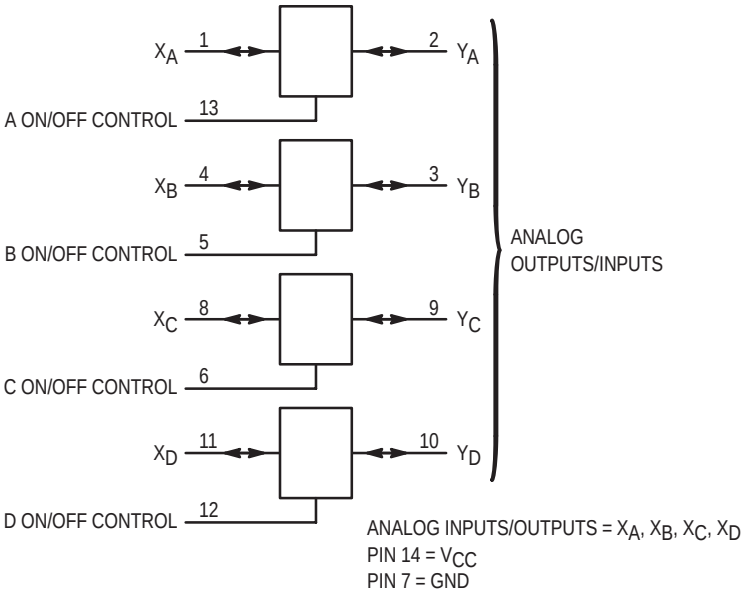
The MC74LVX4066 utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF–channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power–supply range (from V_{CC} to GND).

The LVX4066 is identical in pinout to the metal–gate CMOS MC14066 and the high–speed CMOS HC4066A. Each device has four independent switches. The device has been designed so that the ON resistances (R_{ON}) are much more linear over input voltage than R_{ON} of metal–gate CMOS analog switches.

The ON/OFF control inputs are compatible with standard CMOS outputs; with pull–up resistors, they are compatible with LSTTL outputs.

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power–Supply Voltage Range (V_{CC} – GND) = 2.0 to 6.0 Volts
- Analog Input Voltage Range (V_{CC} – GND) = 2.0 to 6.0 Volts
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14016 or MC14066
- Low Noise
- Chip Complexity: 44 FETs or 11 Equivalent Gates

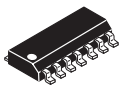
LOGIC DIAGRAM



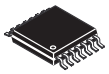
ANALOG INPUTS/OUTPUTS = X_A, X_B, X_C, X_D
PIN 14 = V_{CC}
PIN 7 = GND

ON Semiconductor

http://onsemi.com

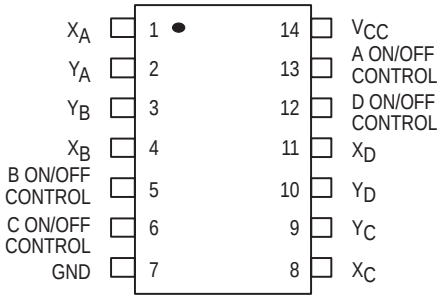


14–LEAD SOIC
D SUFFIX
CASE 751A



14–LEAD TSSOP
DT SUFFIX
CASE 948G

PIN CONNECTION AND MARKING DIAGRAM (Top View)



For detailed package marking information, see the Marking Diagram section on page 140 of this data sheet.

FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On

ORDERING INFORMATION

Device	Package	Shipping
MC74LVX4066D	SOIC	55 Units/Rail
MC74LVX4066DR2	SOIC	2500 Units/Reel
MC74LVX4066DT	TSSOP	96 Units/Rail
MC74LVX4066DTR2	TSSOP	2500 Units/Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{IS}	Analog Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Current Into or Out of ON/OFF Control Pins	± 20	mA
I_S	DC Current Into or Out of Switch Pins	± 20	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IS}	Analog Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch	—	1.2	V
T_A	Operating Temperature, All Package Types	– 55	+ 85	°C
t_r, t_f	Input Rise and Fall Time, ON/OFF Control Inputs (Figure 10) V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

*For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTIC Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Voltage ON/OFF Control Inputs (Note 1)	R_{on} = Per Spec	2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85	1.5 2.1 3.15 3.85	1.5 2.1 3.15 3.85	V
V_{IL}	Maximum Low–Level Voltage ON/OFF Control Inputs (Note 1)	R_{on} = Per Spec	2.0 3.0 4.5 5.5	0.5 0.9 1.35 1.65	0.5 0.9 1.35 1.65	0.5 0.9 1.35 1.65	V
I_{in}	Maximum Input Leakage Current ON/OFF Control Inputs	V_{in} = V_{CC} or GND	5.5V	± 0.1	± 1.0	± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND V_{IO} = 0 V	5.5	4.0	40	160	µA

2. Specifications are for design target only. Not final specification limits.

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
R_{on}	Maximum "ON" Resistance	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ to GND $\|I_S\| \leq 10$ mA (Figures 1, 2)	2.0† 3.0 4.5 5.5	— 40 25 20	— 45 30 25	— 50 35 30	Ω
		$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or GND (Endpoints) $\|I_S\| \leq 10$ mA (Figures 1, 2)	2.0 3.0 4.5 5.5	— 30 25 20	— 35 30 25	— 40 35 30	
ΔR_{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IH}$ V_{IS} = 1/2 (V_{CC} – GND) $I_S \leq 2.0$ mA	3.0 4.5 5.5	15 10 10	20 12 12	25 15 15	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ $V_{IO} = V_{CC}$ or GND Switch Off (Figure 3)	5.5	0.1	0.5	1.0	μA
I_{on}	Maximum On–Channel Leakage Current, Any One Channel	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or GND (Figure 4)	5.5	0.1	0.5	1.0	μA

†At supply voltage (V_{CC}) approaching 2 V the analog switch–on resistance becomes extremely non–linear. Therefore, for low–voltage operation, it is recommended that these devices only be used to control digital signals (See Figure 1a).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, ON/OFF Control Inputs: $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0 3.0 4.5 5.5	4.0 3.0 1.0 1.0	6.0 5.0 2.0 2.0	8.0 6.0 2.0 2.0	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0 3.0 4.5 5.5	30 20 15 15	35 25 18 18	40 30 22 20	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 1 1)	2.0 3.0 4.5 5.5	20 12 8.0 8.0	25 14 10 10	30 15 12 12	ns
C	Maximum Capacitance — ON/OFF Control Input	—	10	10	10	pF
	Control Input = GND Analog I/O Feedthrough	 — —	 35 1.0	 35 1.0	 35 1.0	

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Switch) (Figure 13)*	15	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Test Conditions	V_{CC} V	Limit* 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 5)	f_{in} = 1 MHz Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{OS} Increase f_{in} Frequency Until dB Meter Reads – 3 dB R_L = 50 Ω, C_L = 10 pF	4.5 5.5	150 160	MHz
—	Off–Channel Feedthrough Isolation (Figure 6)	$f_{in} \equiv$ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	4.5 5.5	– 50 – 50	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	4.5 5.5	– 37 – 37	
—	Feedthrough Noise, Control to Switch (Figure 7)	$V_{in} \leq$ 1 MHz Square Wave ($t_r = t_f$ = 6 ns) Adjust R_L at Setup so that I_S = 0 A R_L = 600 Ω, C_L = 50 pF	4.5 5.5	100 200	mV_{PP}
		R_L = 10 kΩ, C_L = 10 pF	4.5 5.5	50 100	
—	Crosstalk Between Any Two Switches (Figure 12)	$f_{in} \equiv$ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	4.5 5.5	– 70 – 70	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	4.5 5.5	– 80 – 80	
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1 kHz, R_L = 10 kΩ, C_L = 50 pF $THD = THD_{Measured} - THD_{Source}$ V_{IS} = 4.0 V_{PP} sine wave V_{IS} = 5.0 V_{PP} sine wave	 4.5 5.5	 0.10 0.06	%

*Guaranteed limits not tested. Determined by design and verified by qualification.

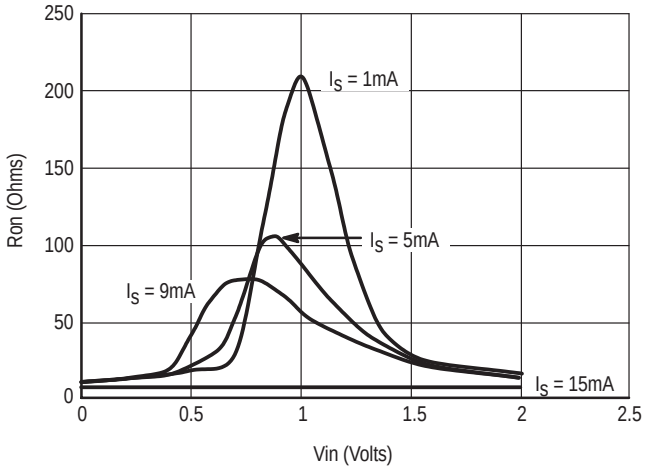


Figure 1a. Typical On Resistance, V_{CC} = 2.0 V, T = 25°C

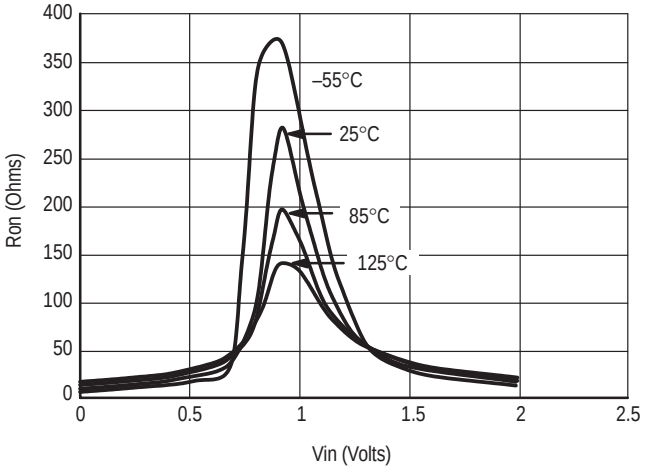


Figure 1b. Typical On Resistance, V_{CC} = 2.0 V

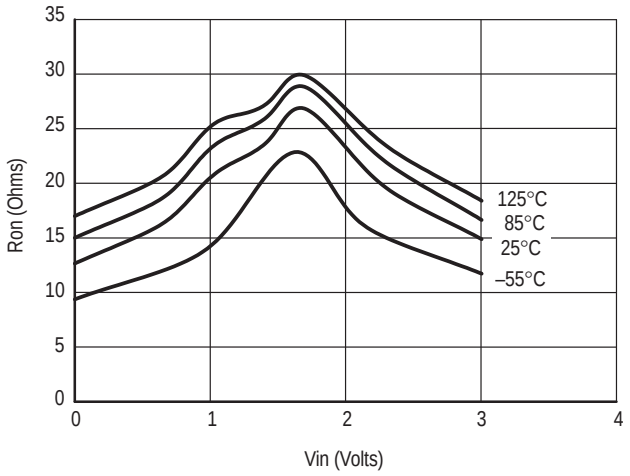


Figure 1c. Typical On Resistance, V_{CC} = 3.0 V

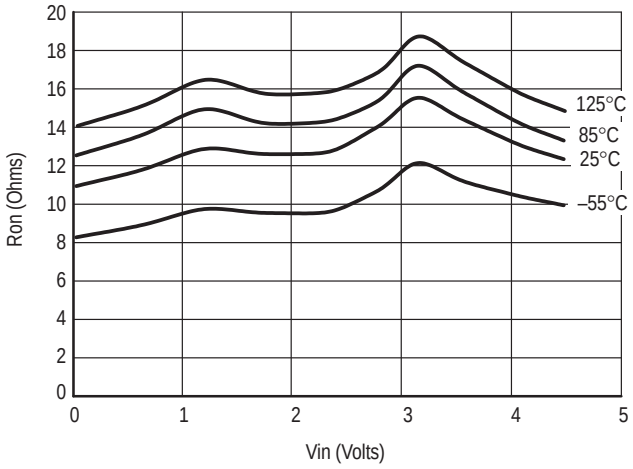


Figure 1d. Typical On Resistance, V_{CC} = 4.5 V

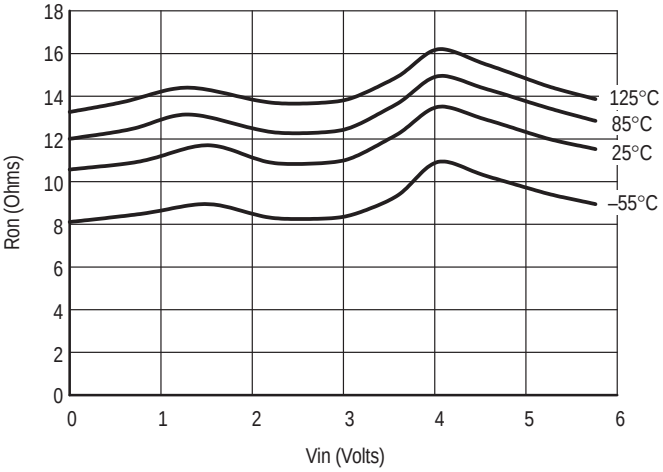


Figure 1e. Typical On Resistance, V_{CC} = 5.5 V

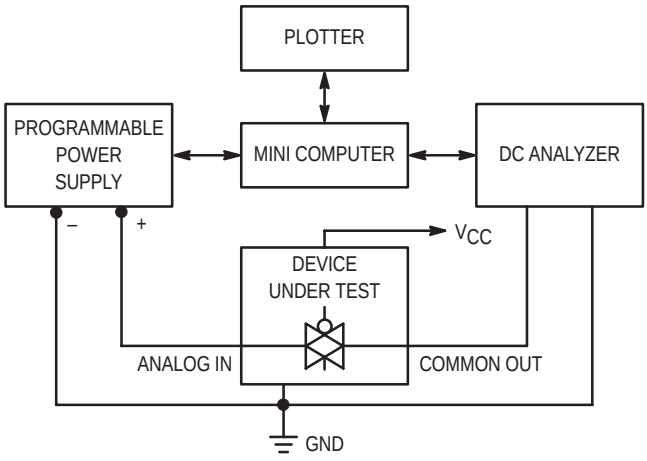


Figure 2. On Resistance Test Set–Up

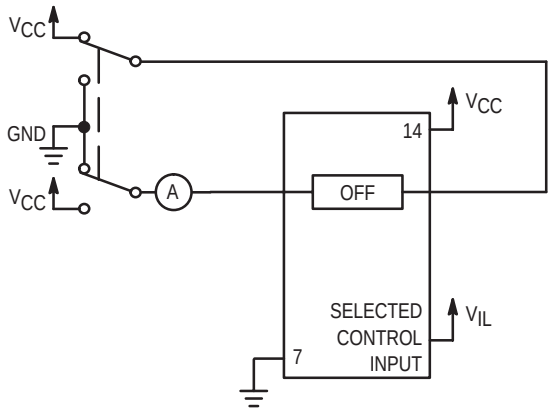


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

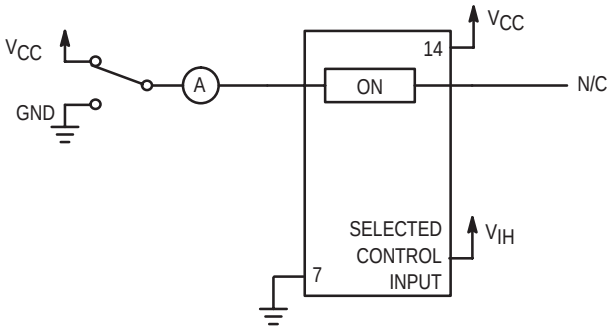
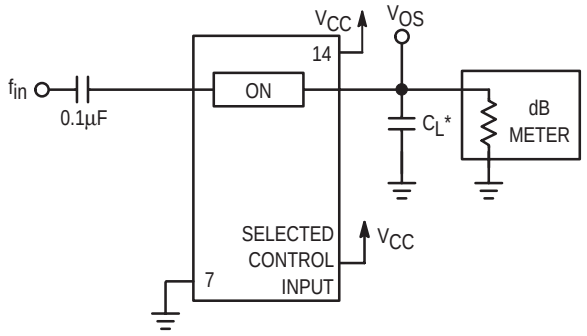
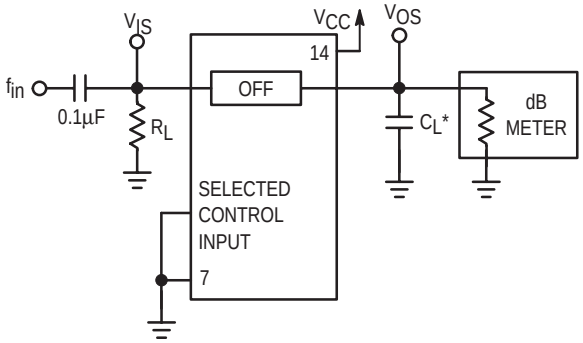


Figure 4. Maximum On Channel Leakage Current, Test Set–Up



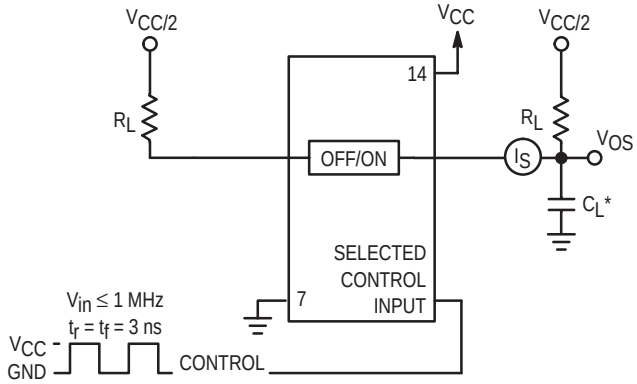
*Includes all probe and jig capacitance.

Figure 5. Maximum On–Channel Bandwidth Test Set–Up



*Includes all probe and jig capacitance.

Figure 6. Off–Channel Feedthrough Isolation, Test Set–Up



*Includes all probe and jig capacitance.

Figure 7. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set–Up

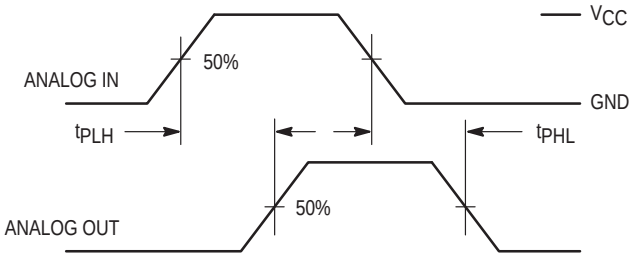
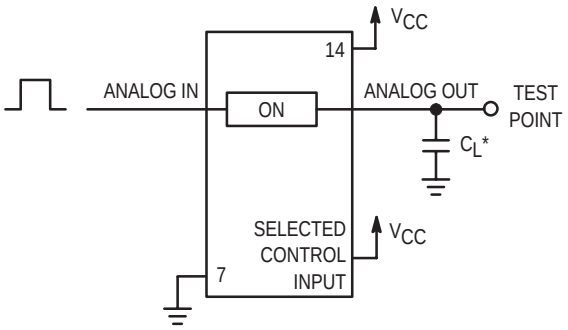


Figure 8. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set–Up

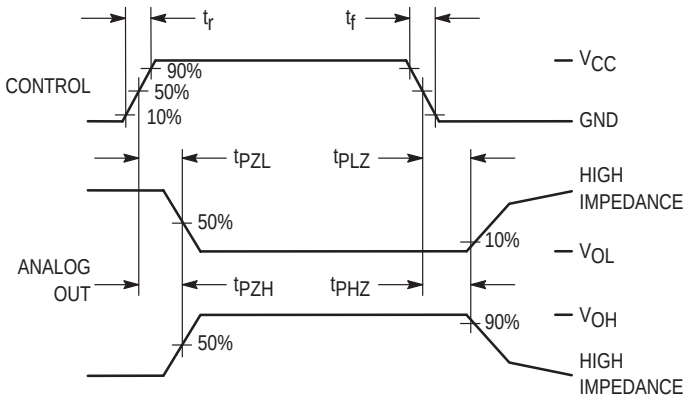
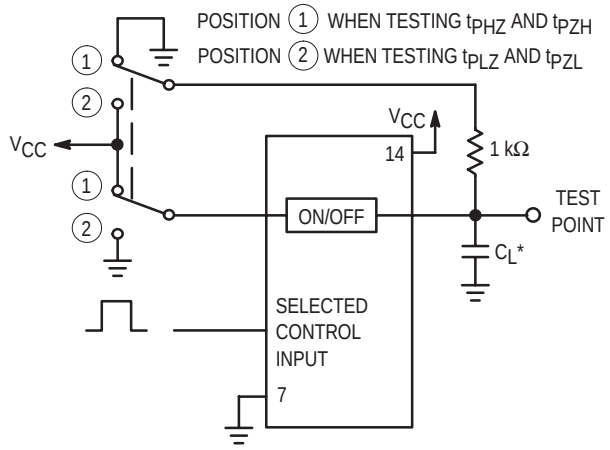
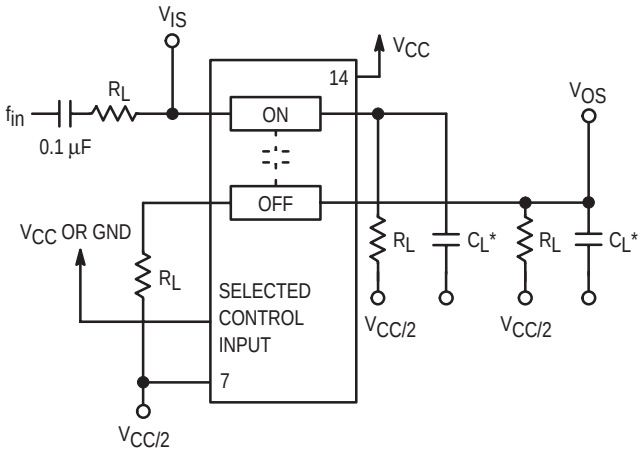


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set–Up



*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set–Up

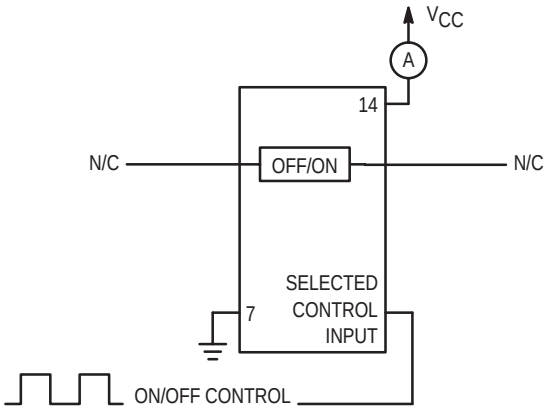
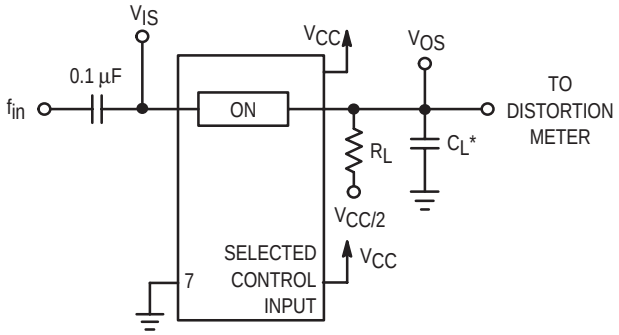


Figure 13. Power Dissipation Capacitance Test Set–Up



*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set–Up

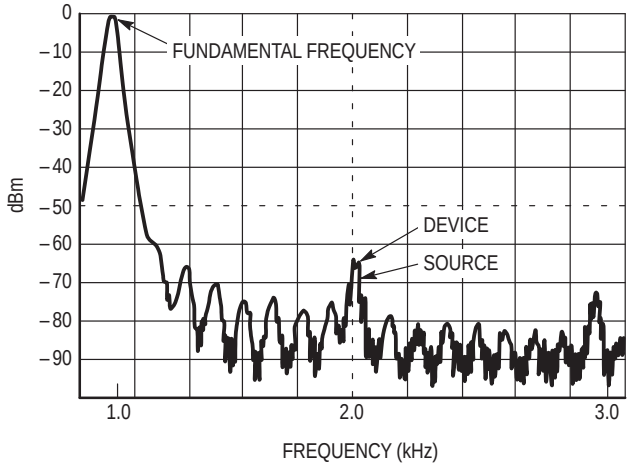


Figure 15. Plot, Harmonic Distortion

APPLICATION INFORMATION

The ON/OFF Control pins should be at V_{CC} or GND logic levels, V_{CC} being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to V_{CC} or GND through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked–up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages V_{CC} and GND. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below GND. In the example below, the difference between V_{CC} and GND is six volts. Therefore, using the configuration in Figure 16, a maximum analog signal of six volts peak–to–peak can be controlled.

When voltage transients above V_{CC} and/or below GND are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure 17. These diodes should be small signal, fast turn–on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the Dx diodes with Mosorbs (Mosorb™ is an acronym for high current surge protectors). Mosorbs are fast turn–on devices ideally suited for precise DC protection with no inherent wear out mechanism.

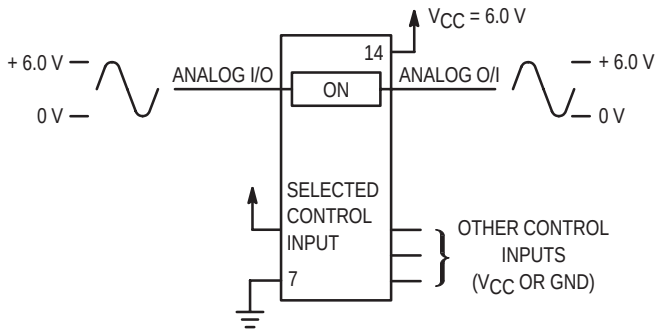


Figure 16. 6.0 V Application

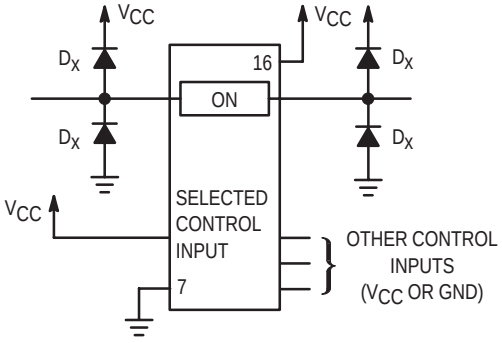
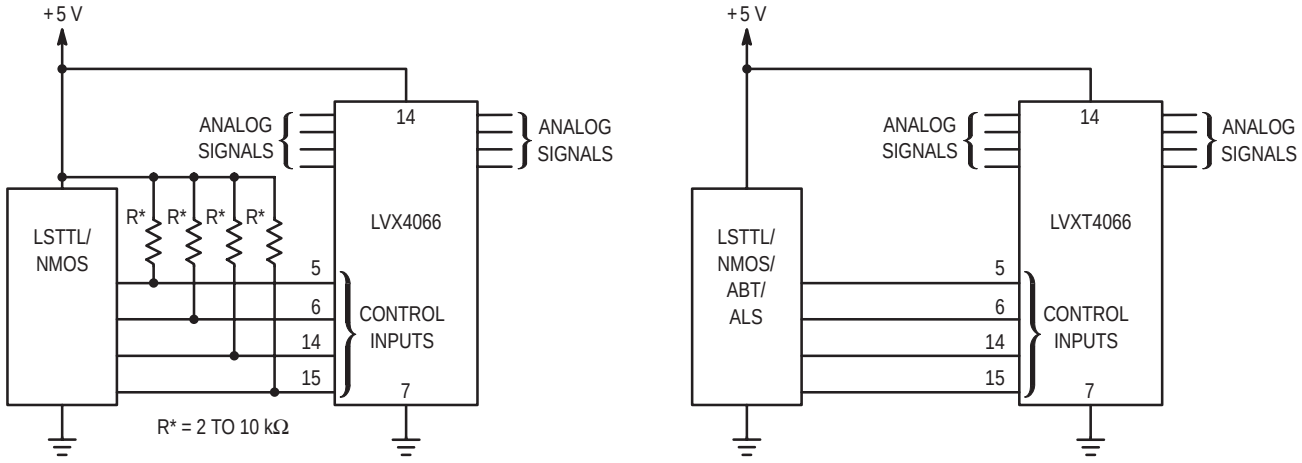


Figure 17. Transient Suppressor Application



a. Using Pull-Up Resistors **b. Using LVXT4066**

Figure 18. LSTTL/NMOS to CMOS Interface

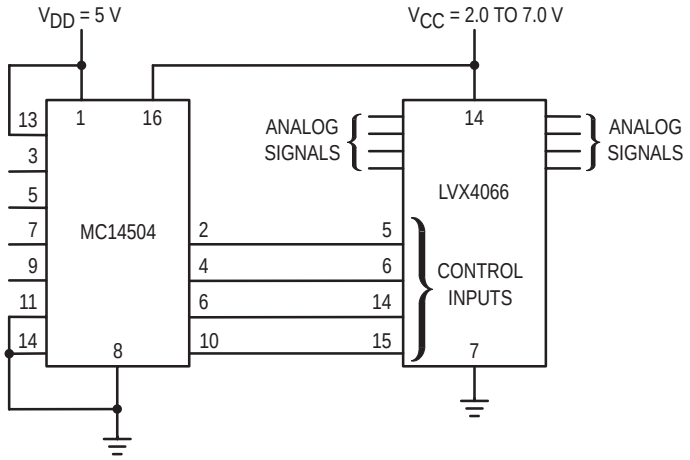


Figure 19. TTL/NMOS–to–CMOS Level Converter Analog Signal Peak–to–Peak Greater than 5 V

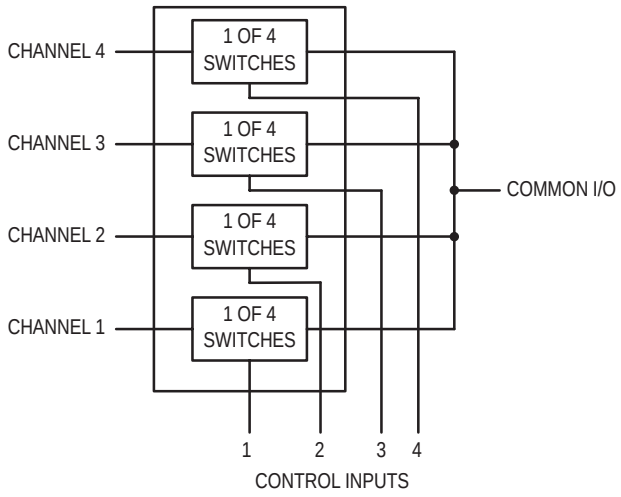


Figure 20. 4–Input Multiplexer

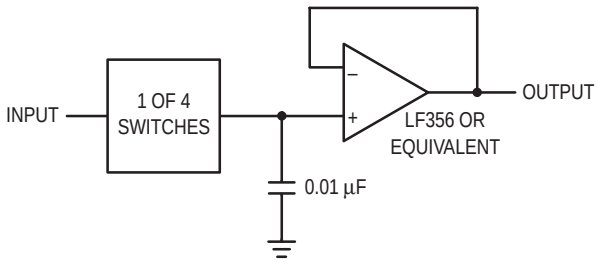
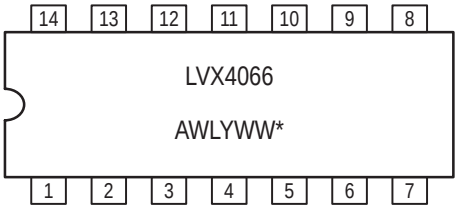
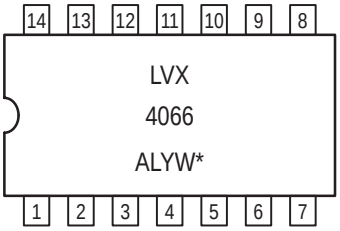


Figure 21. Sample/Hold Amplifier

MARKING DIAGRAMS
(Top View)



14–LEAD SOIC
D SUFFIX
CASE 751A



14–LEAD TSSOP
DT SUFFIX
CASE 948G

*See Applications Note #AND8004/D for date code and traceability information.

MC74LVXT4066

Quad Analog Switch/ Multiplexer/Demultiplexer

High–Performance Silicon–Gate CMOS

The MC74LVXT4066 utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF–channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power–supply range (from V_{CC} to GND).

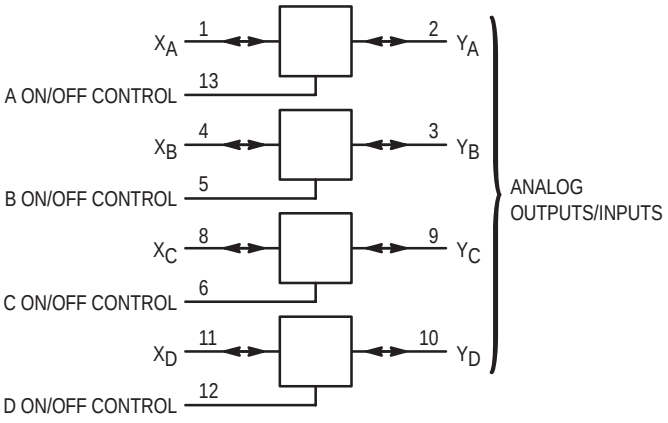
The LVXT4066 is identical in pinout to the metal–gate CMOS MC14066 and the high–speed CMOS HC4066A. Each device has four independent switches. The device has been designed so that the ON resistances (R_{ON}) are much more linear over input voltage than R_{ON} of metal–gate CMOS analog switches.

The ON/OFF control inputs are compatible with standard LSTTL outputs. The input protection circuitry on this device allows overvoltage tolerance on the ON/OFF control inputs, allowing the device to be used as a logic–level translator from 3.0V CMOS logic to 5.0V CMOS Logic or from 1.8V CMOS logic to 3.0V CMOS Logic while operating at the higher–voltage power supply.

The MC74LVXT4066 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74LVXT4066 to be used to interface 5V circuits to 3V circuits.

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power–Supply Voltage Range (V_{CC} – GND) = 2.0 to 6.0 Volts
- Analog Input Voltage Range (V_{CC} – GND) = 2.0 to 6.0 Volts
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14016 or MC14066
- Low Noise

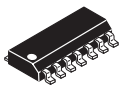
LOGIC DIAGRAM



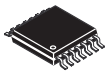
ANALOG INPUTS/OUTPUTS = X_A, X_B, X_C, X_D
PIN 14 = V_{CC}
PIN 7 = GND

ON Semiconductor

http://onsemi.com

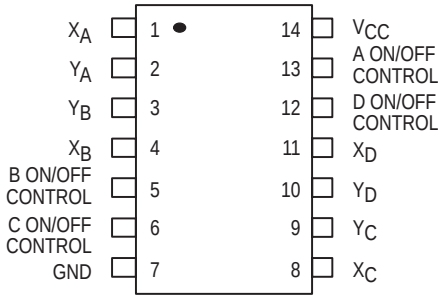


14–LEAD SOIC
D SUFFIX
CASE 751A



14–LEAD TSSOP
DT SUFFIX
CASE 948G

PIN CONNECTION AND MARKING DIAGRAM (Top View)



For detailed package marking information, see the Marking Diagram section on page 150 of this data sheet.

FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On

ORDERING INFORMATION

Device	Package	Shipping
MC74LVXT4066D	SOIC	55 Units/Rail
MC74LVXT4066DR2	SOIC	2500 Units/Reel
MC74LVXT4066DT	TSSOP	96 Units/Rail
MC74LVXT4066DTR2	TSSOP	2500 Units/Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{IS}	Analog Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current Into or Out of Any Pin	–20	mA
P_D	Power Dissipation in Still Air, SOIC Package†	500	mW
	TSSOP Package†	450	
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	2.0	5.5	V
V_{IS}	Analog Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch	—	1.2	V
T_A	Operating Temperature, All Package Types	– 55	+ 85	°C
t_r, t_f	Input Rise and Fall Time, ON/OFF Control			ns/V
	Inputs (Figure 10) V_{CC} = 3.3 V ± 0.3 V	0	100	
	V_{CC} = 5.0 V ± 0.5 V	0	20	

*For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTIC Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Voltage ON/OFF Control Inputs (Note 1)	R_{on} = Per Spec	3.0 4.5 5.5	1.2 2.0 2.0	1.2 2.0 2.0	1.2 2.0 2.0	V
V_{IL}	Maximum Low–Level Voltage ON/OFF Control Inputs (Note 1)	R_{on} = Per Spec	3.0 4.5 5.5	0.53 0.8 0.8	0.53 0.8 0.8	0.53 0.8 0.8	V
I_{in}	Maximum Input Leakage Current ON/OFF Control Inputs	V_{in} = V_{CC} or GND	5.5	± 0.1	± 1.0	± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND V_{IO} = 0 V	5.5	4.0	40	160	µA

3. Specifications are for design target only. Not final specification limits.

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
R_{on}	Maximum "ON" Resistance	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ to GND $I_S \leq 2.0$ mA (Figures 1, 2)	2.0† 3.0 4.5 5.5	— 40 25 20	— 45 28 25	— 50 35 30	Ω
		$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or GND (Endpoints) $I_S \leq 2.0$ mA (Figures 1, 2)	2.0 3.0 4.5 5.5	— 30 25 20	— 35 28 25	— 40 35 30	
ΔR_{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IH}$ V_{IS} = 1/2 (V_{CC} – GND) $I_S \leq 2.0$ mA	3.0 4.5 5.5	15 10 10	20 12 12	25 15 15	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ $V_{IO} = V_{CC}$ or GND Switch Off (Figure 3)	5.5	0.1	0.5	1.0	μA
I_{on}	Maximum On–Channel Leakage Current, Any One Channel	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or GND (Figure 4)	5.5	0.1	0.5	1.0	μA

†At supply voltage (V_{CC}) approaching 2 V the analog switch–on resistance becomes extremely non–linear. Therefore, for low–voltage operation, it is recommended that these devices only be used to control digital signals.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, ON/OFF Control Inputs: $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0 3.0 4.5 5.5	4.0 3.0 1.0 1.0	6.0 5.0 2.0 2.0	8.0 6.0 2.0 2.0	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0 3.0 4.5 5.5	30 20 15 15	35 25 18 18	40 30 22 20	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 1 1)	2.0 3.0 4.5 5.5	20 12 8.0 8.0	25 14 10 10	30 15 12 12	ns
C	Maximum Capacitance — ON/OFF Control Input	—	10	10	10	pF
	Control Input = GND Analog I/O Feedthrough	 — —	 35 1.0	 35 1.0	 35 1.0	

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Switch) (Figure 13)*	15	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Test Conditions	V_{CC} V	Limit* 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 5)	f_{in} = 1 MHz Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{OS} Increase f_{in} Frequency Until dB Meter Reads – 3 dB R_L = 50 Ω, C_L = 10 pF	4.5 5.5	150 160	MHz
—	Off–Channel Feedthrough Isolation (Figure 6)	$f_{in} \equiv$ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	4.5 5.5	– 50 – 50	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	4.5 5.5	– 37 – 37	
—	Feedthrough Noise, Control to Switch (Figure 7)	$V_{in} \leq$ 1 MHz Square Wave ($t_r = t_f$ = 3 ns) Adjust R_L at Setup so that I_S = 0 A R_L = 600 Ω, C_L = 50 pF	4.5 5.5	100 200	mV_{PP}
		R_L = 10 kΩ, C_L = 10 pF	4.5 5.5	50 100	
—	Crosstalk Between Any Two Switches (Figure 12)	$f_{in} \equiv$ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	4.5 5.5	– 70 – 70	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	4.5 5.5	– 80 – 80	
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1 kHz, R_L = 10 kΩ, C_L = 50 pF $THD = THD_{Measured} - THD_{Source}$ V_{IS} = 4.0 V_{PP} sine wave V_{IS} = 5.0 V_{PP} sine wave	 4.5 5.5	 0.10 0.06	%

*Guaranteed limits not tested. Determined by design and verified by qualification.

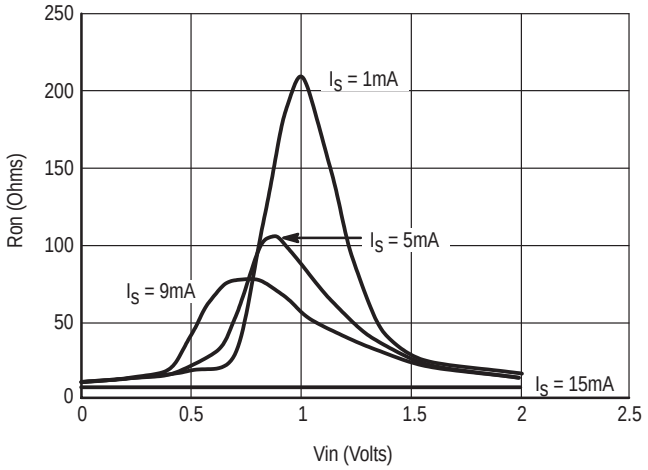


Figure 1a. Typical On Resistance, V_{CC} = 2.0 V, T = 25°C

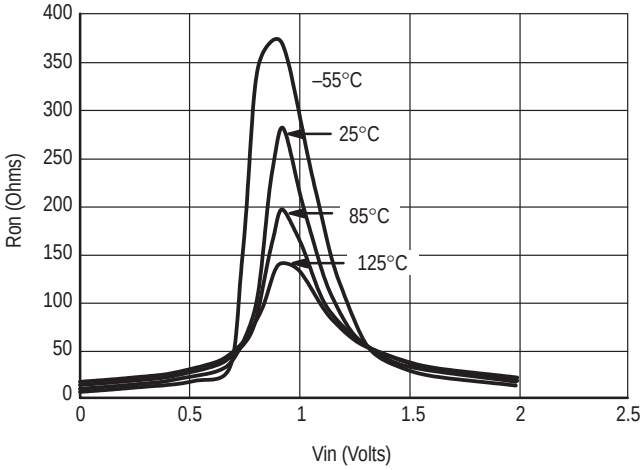


Figure 1b. Typical On Resistance, V_{CC} = 2.0 V

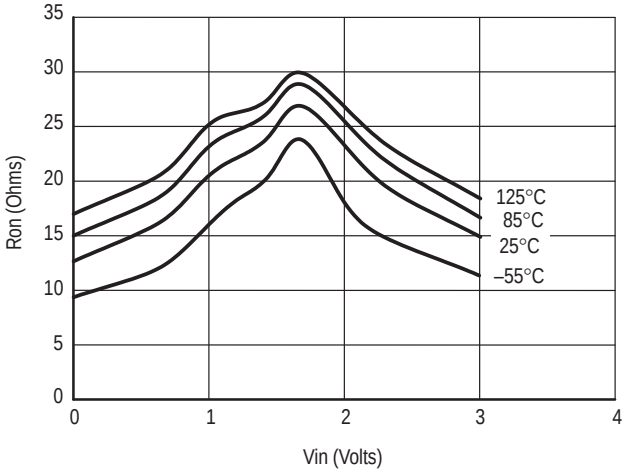


Figure 1c. Typical On Resistance, V_{CC} = 3.0 V

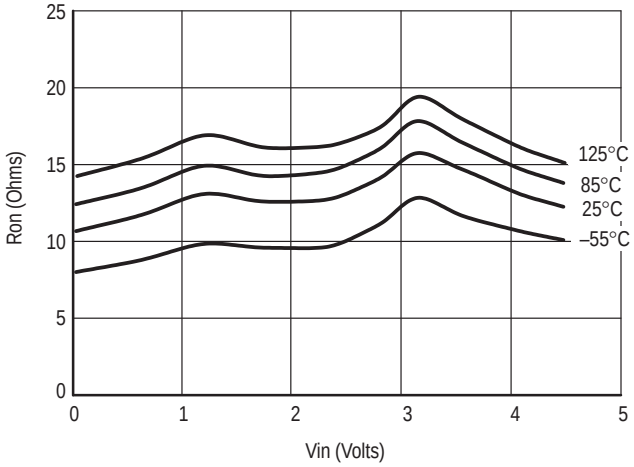


Figure 1d. Typical On Resistance, V_{CC} = 4.5 V

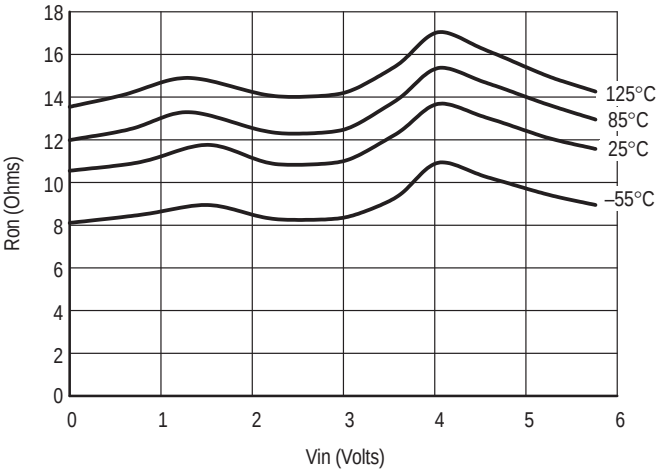


Figure 1e. Typical On Resistance, V_{CC} = 5.5 V

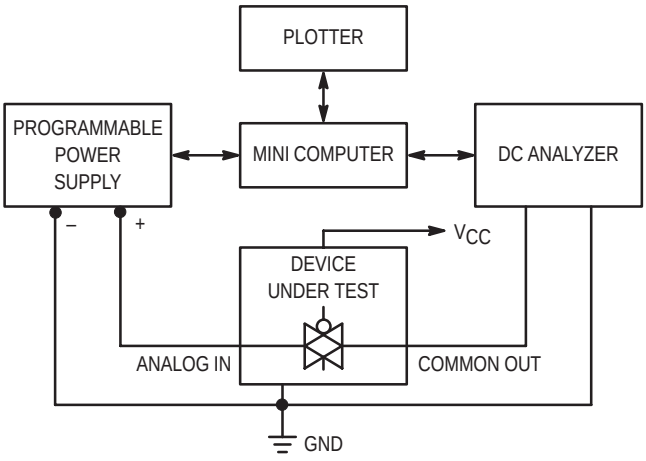


Figure 2. On Resistance Test Set–Up

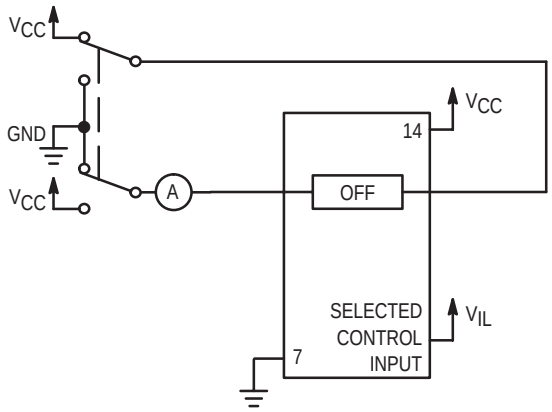


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

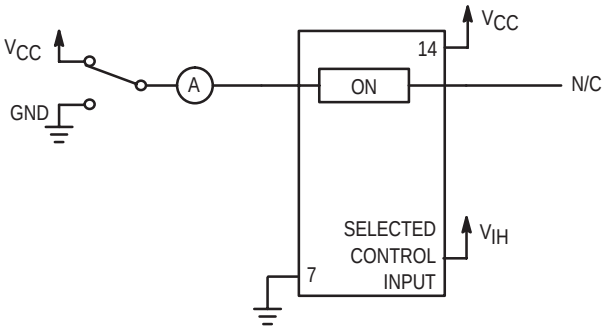
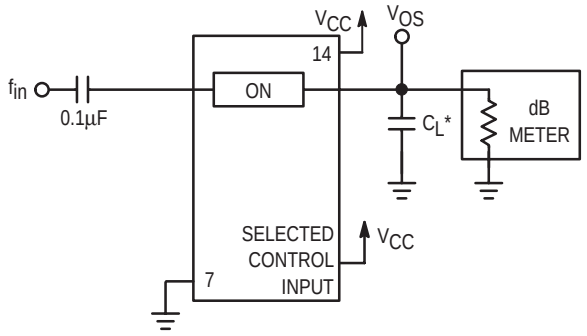
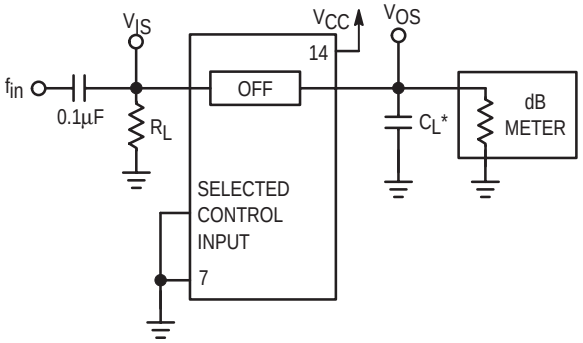


Figure 4. Maximum On Channel Leakage Current, Test Set–Up



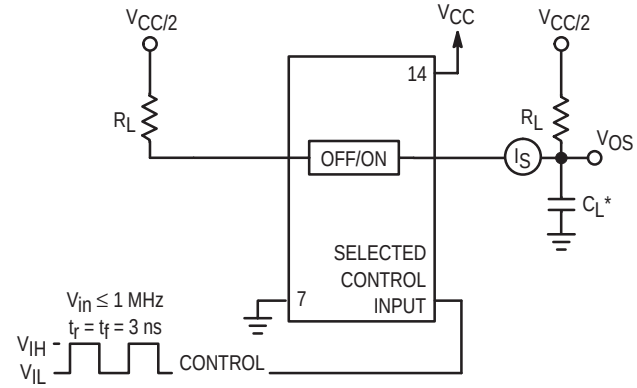
*Includes all probe and jig capacitance.

Figure 5. Maximum On–Channel Bandwidth Test Set–Up



*Includes all probe and jig capacitance.

Figure 6. Off–Channel Feedthrough Isolation, Test Set–Up



*Includes all probe and jig capacitance.

Figure 7. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set–Up

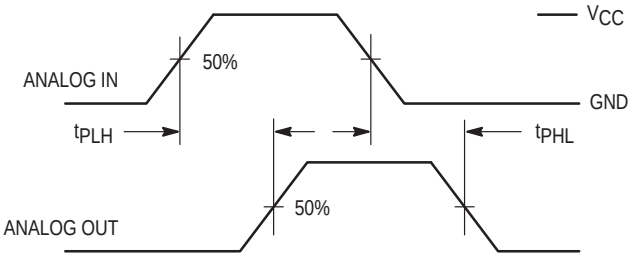
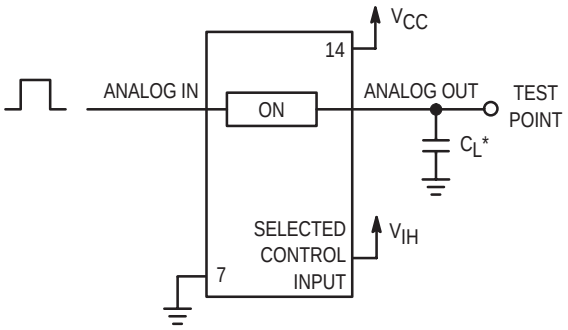


Figure 8. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set–Up

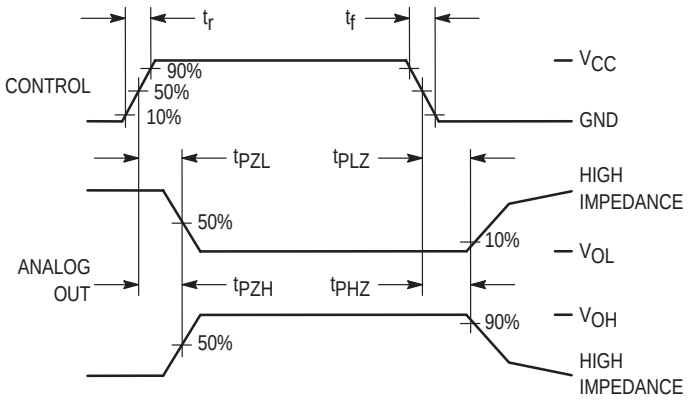
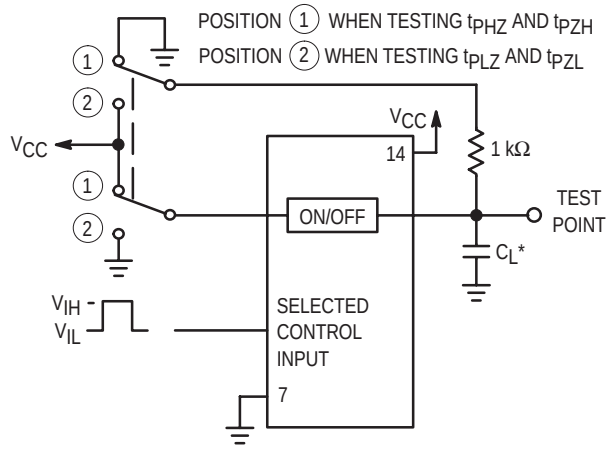
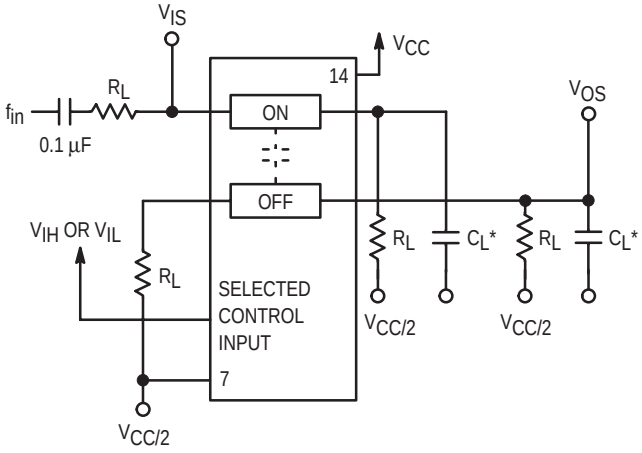


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set–Up



*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set–Up

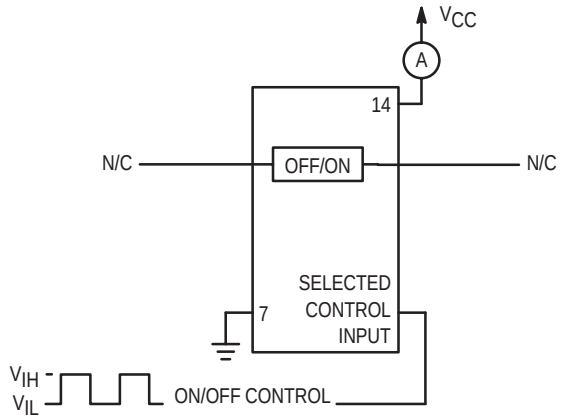
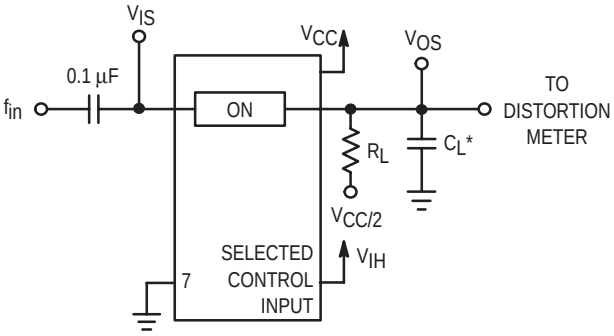


Figure 13. Power Dissipation Capacitance Test Set–Up



*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set–Up

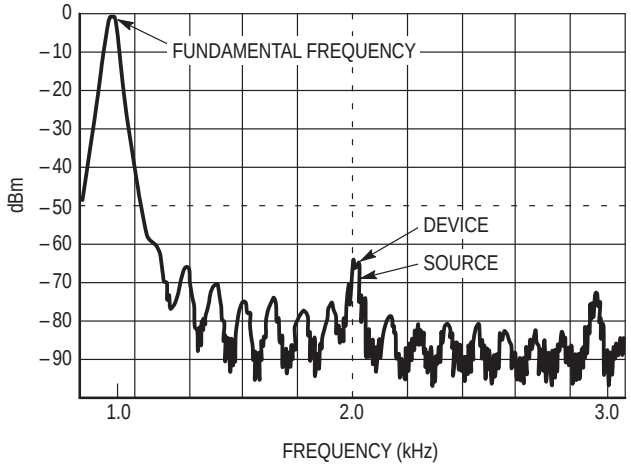


Figure 15. Plot, Harmonic Distortion

APPLICATION INFORMATION

The ON/OFF Control pins should be at V_{IH} or V_{IL} logic levels, V_{IH} being recognized as logic high and V_{IL} being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to V_{CC} or GND through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked–up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages V_{CC} and GND. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below GND. In the example below, the difference between V_{CC} and GND is six volts. Therefore, using the configuration in Figure 16, a maximum analog signal of six volts peak–to–peak can be controlled.

When voltage transients above V_{CC} and/or below GND are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure 17. These diodes should be small signal, fast turn–on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the Dx diodes with Mosorbs (Mosorb™ is an acronym for high current surge protectors). Mosorbs are fast turn–on devices ideally suited for precise DC protection with no inherent wear out mechanism.

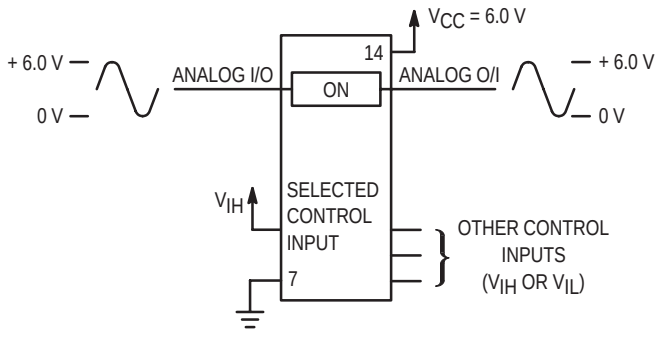


Figure 16. 6.0 V Application

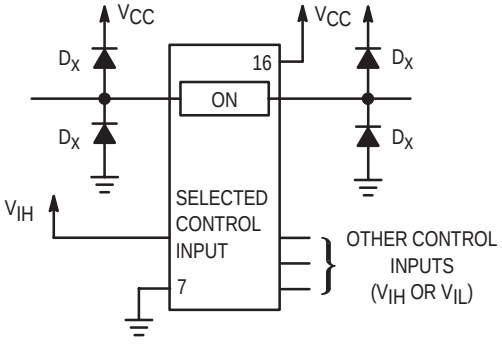
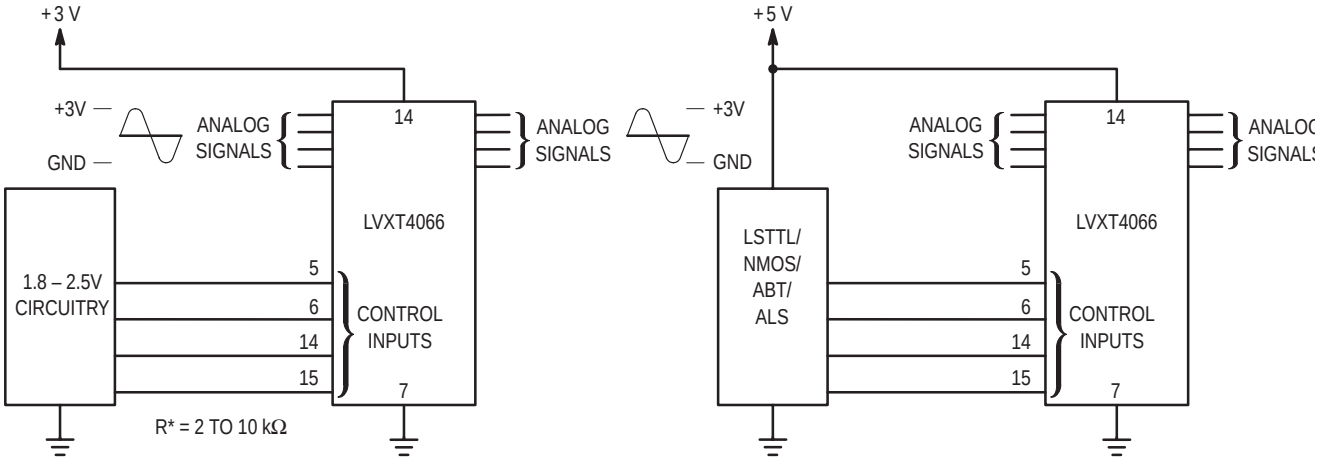


Figure 17. Transient Suppressor Application



a. Low Voltage Logic Level Shifting Control **b. Using LVXT4066**

Figure 18. Low Voltage CMOS Interface

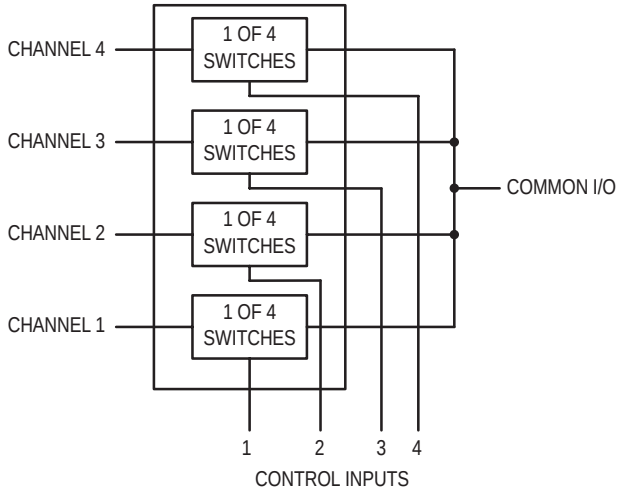


Figure 19. 4–Input Multiplexer

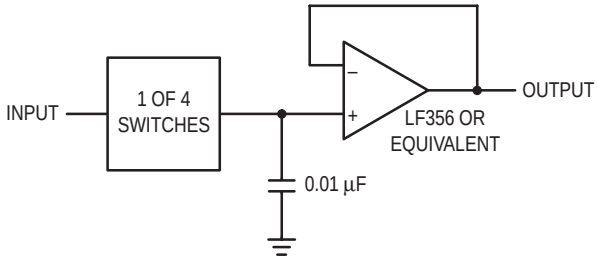
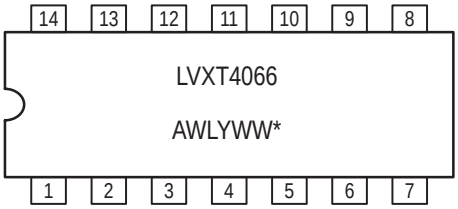
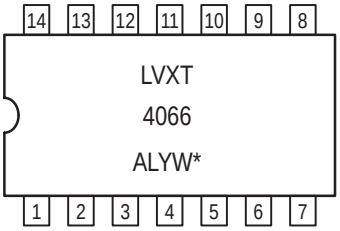


Figure 20. Sample/Hold Amplifier

MARKING DIAGRAMS
(Top View)



14–LEAD SOIC
D SUFFIX
CASE 751A



14–LEAD TSSOP
DT SUFFIX
CASE 948G

*See Applications Note #AND8004/D for date code and traceability information.

MC74LVX8051

Analog Multiplexer / Demultiplexer

High–Performance Silicon–Gate CMOS

The MC74LVX8051 utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to GND).

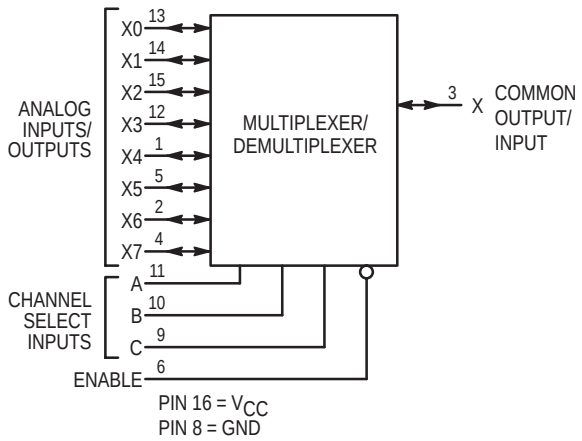
The LVX8051 is similar in pinout to the high–speed HC4051A and the metal–gate MC14051B. The Channel–Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel–Select and Enable inputs are compatible with standard CMOS outputs; with pull–up resistors they are compatible with LSTTL outputs.

This device has been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal–gate CMOS analog switches.

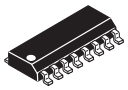
- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Digital (Control) Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal–Gate Counterparts
- Low Noise
- In Compliance With the Requirements of JEDEC Standard No. 7A
- Chip Complexity: LVX8051 — 184 FETs or 46 Equivalent Gates

LOGIC DIAGRAM
MC74LVX8051
Single–Pole, 8–Position Plus Common Off

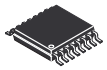


ON Semiconductor

http://onsemi.com

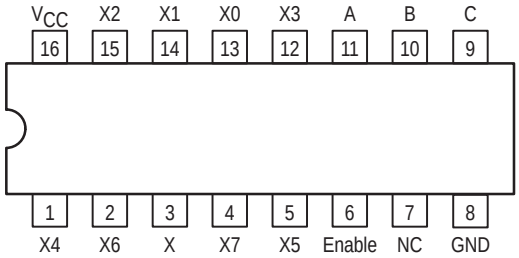


16–LEAD SOIC
D SUFFIX
CASE 751B



16–LEAD TSSOP
DT SUFFIX
CASE 948F

PIN CONNECTION AND MARKING DIAGRAM (Top View)



For detailed package marking information, see the Marking Diagram section on page 161 of this data sheet.

FUNCTION TABLE – MC74LVX8051

Control Inputs				
	Select			
Enable	C	B	A	ON Channels
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

X = Don't Care

ORDERING INFORMATION

Device	Package	Shipping
MC74LVX8051D	SOIC	48 Units/Rail
MC74LVX8051DR2	SOIC	2500 Units/Reel
MC74LVX8051DT	TSSOP	96 Units/Rail
MC74LVX8051DTR2	TSSOP	2500 Units/Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{IS}	Analog Input Voltage	– 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin	± 20	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IS}	Analog Input Voltage	0.0	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		1.2	V
T_A	Operating Temperature Range, All Package Types	– 55	+ 85	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs) V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	 0 0	 100 20	ns/V

*For voltage drops across switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 5.5	1.50 2.10 3.15 3.85	1.50 2.10 3.15 3.85	1.50 2.10 3.15 3.85	V
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 5.5	0.5 0.9 1.35 1.65	0.5 0.9 1.35 1.65	0.5 0.9 1.35 1.65	V
I_{in}	Maximum Input Leakage Current, Channel–Select or Enable Inputs	V_{in} = V_{CC} or GND	5.5	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and V_{IS} = V_{CC} or GND; V_{IO} = 0 V	5.5	4.0	40	160	μA

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
R_{on}	Maximum “ON” Resistance	V_{in} = V_{IL} or V_{IH} V_{IS} = V_{CC} to GND $\|I_S\|$ ≤ 10.0 mA (Figures 1, 2)	3.0 4.5 5.5	40 30 25	45 32 28	50 37 30	Ω
		V_{in} = V_{IL} or V_{IH} V_{IS} = V_{CC} or GND (Endpoints) $\|I_S\|$ ≤ 10.0 mA (Figures 1, 2)	3.0 4.5 5.5	30 25 20	35 28 25	40 35 30	
ΔR_{on}	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	V_{in} = V_{IL} or V_{IH} V_{IS} = 1/2 (V_{CC} – GND) $\|I_S\|$ ≤ 10.0 mA	3.0 4.5 5.5	15 8.0 8.0	20 12 12	25 15 15	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} or GND; Switch Off (Figure 3)	5.5	0.1	0.5	1.0	μA
	Maximum Off–Channel Leakage Current, Common Channel	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} or GND; Switch Off (Figure 4)	5.5	0.2	2.0	4.0	
I_{on}	Maximum On–Channel Leakage Current, Channel–to–Channel	V_{in} = V_{IL} or V_{IH}; Switch–to–Switch = V_{CC} or GND; (Figure 5)	5.5	0.2	2.0	4.0	μA

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 3 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Channel–Select to Analog Output (Figure 9)	2.0 3.0 4.5 5.5	30 20 15 15	35 25 18 18	40 30 22 20	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0 3.0 4.5 5.5	4.0 3.0 1.0 1.0	6.0 5.0 2.0 2.0	8.0 6.0 2.0 2.0	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 5.5	30 20 15 15	35 25 18 18	40 30 22 20	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 5.5	20 12 8.0 8.0	25 14 10 10	30 15 12 12	ns
C_{in}	Maximum Input Capacitance, Channel–Select or Enable Inputs		10	10	10	pF
$C_{I/O}$	Maximum Capacitance Analog I/O		35	35	35	pF
	(All Switches Off) Common O/I		130	130	130	
	Feedthrough		1.0	1.0	1.0	

C_{PD}		**Typical @ 25°C, V_{CC} = 5.0 V**	pF
	Power Dissipation Capacitance (Figure 13)*	45	

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V_{CC} V	Limit* 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 6)	f_{in} = 1MHz Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{OS}; Increase f_{in} Frequency Until dB Meter Reads –3dB; R_L = 50Ω, C_L = 10pF	3.0 4.5 5.5	80 80 80	MHz
—	Off–Channel Feedthrough Isolation (Figure 7)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600Ω, C_L = 50pF	3.0 4.5 5.5	–50 –50 –50	dB
		f_{in} = 1.0MHz, R_L = 50Ω, C_L = 10pF	3.0 4.5 5.5	–37 –37 –37	
—	Feedthrough Noise. Channel–Select Input to Common I/O (Figure 8)	$V_{in} \leq$ 1MHz Square Wave ($t_r = t_f$ = 6ns); Adjust R_L at Setup so that I_S = 0A; Enable = GND R_L = 600Ω, C_L = 50pF	3.0 4.5 5.5	25 105 135	mV_{PP}
		R_L = 10kΩ, C_L = 10pF	3.0 4.5 5.5	35 145 190	
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1kHz, R_L = 10kΩ, C_L = 50pF THD = $THD_{measured} - THD_{source}$ V_{IS} = 2.0V_{PP} sine wave V_{IS} = 4.0V_{PP} sine wave V_{IS} = 5.0V_{PP} sine wave	 3.0 4.5 5.5	 0.10 0.08 0.05	%

*Limits not tested. Determined by design and verified by qualification.

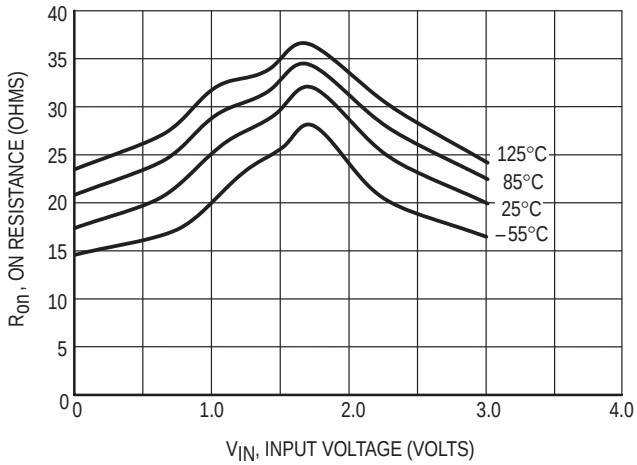


Figure 1a. Typical On Resistance, V_{CC} = 3.0 V

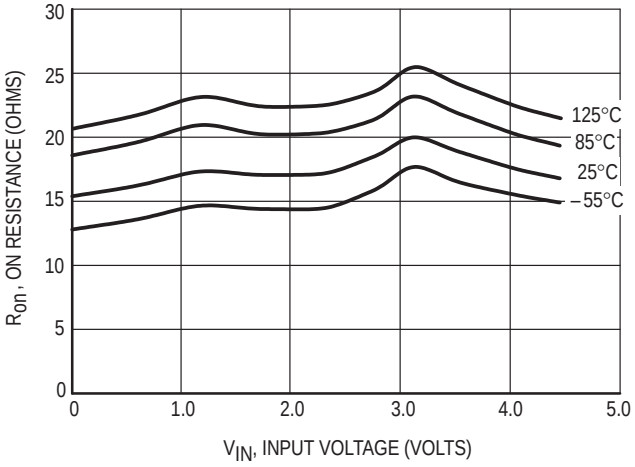


Figure 1b. Typical On Resistance, V_{CC} = 4.5 V

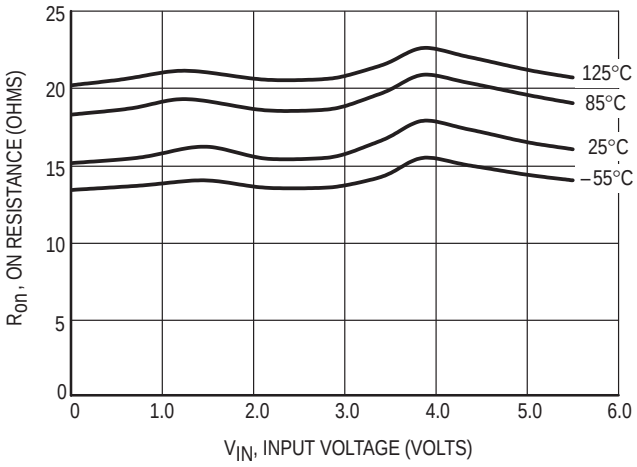


Figure 1c. Typical On Resistance, V_{CC} = 5.5 V

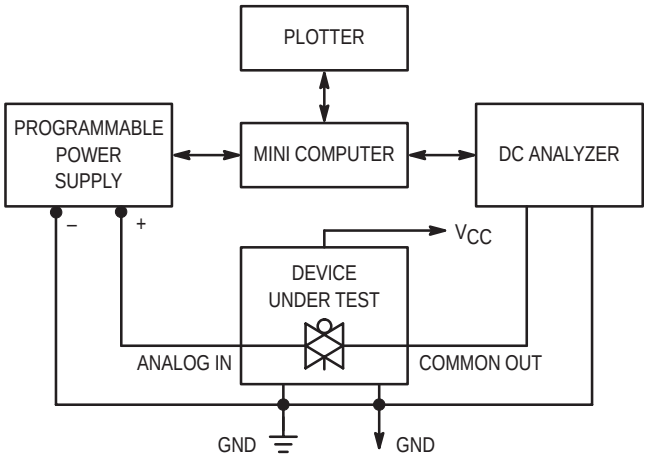


Figure 2. On Resistance Test Set–Up

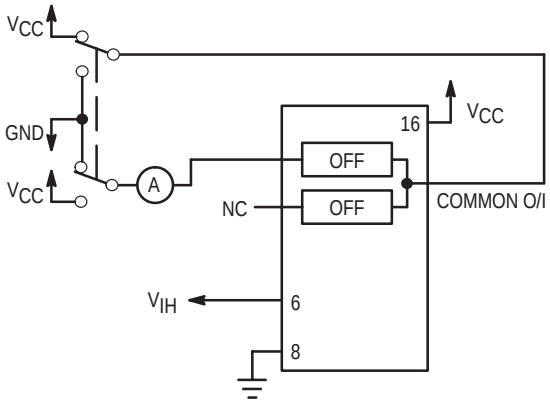


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

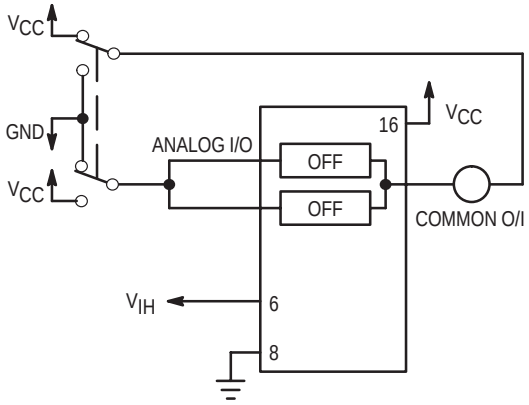


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set–Up

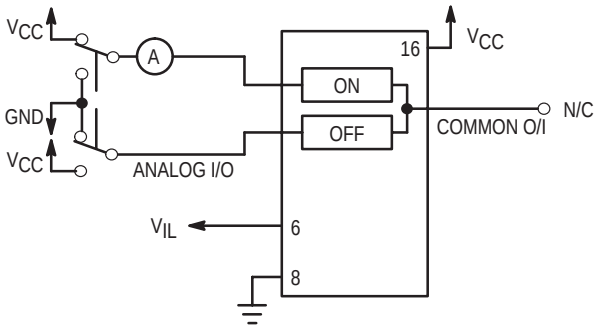
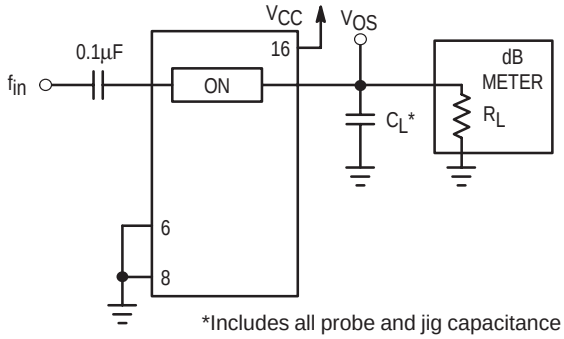
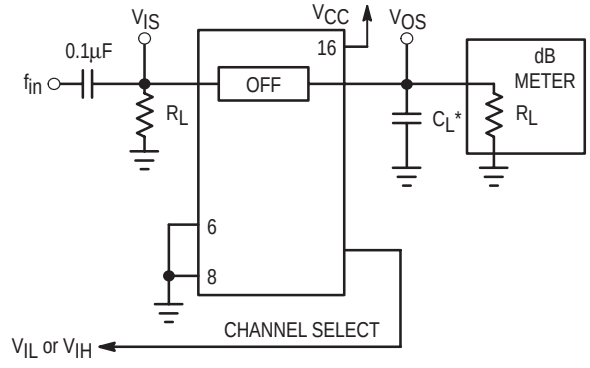


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set–Up



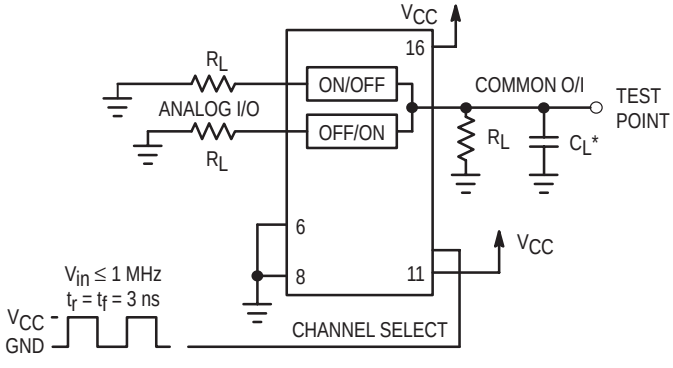
*Includes all probe and jig capacitance

Figure 6. Maximum On Channel Bandwidth, Test Set–Up



*Includes all probe and jig capacitance

Figure 7. Off Channel Feedthrough Isolation, Test Set–Up



*Includes all probe and jig capacitance

Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set–Up

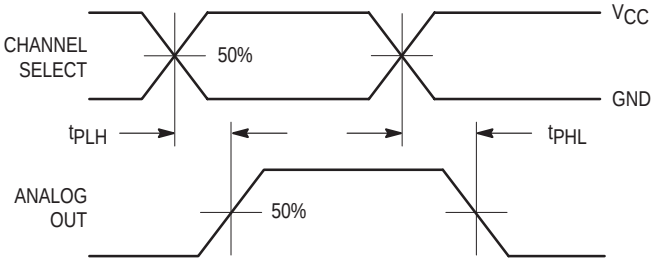
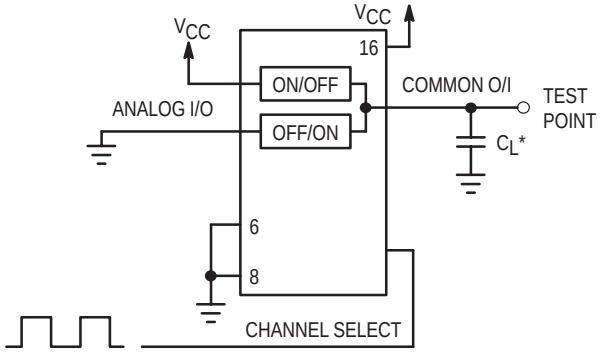


Figure 9a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 9b. Propagation Delay, Test Set–Up Channel Select to Analog Out

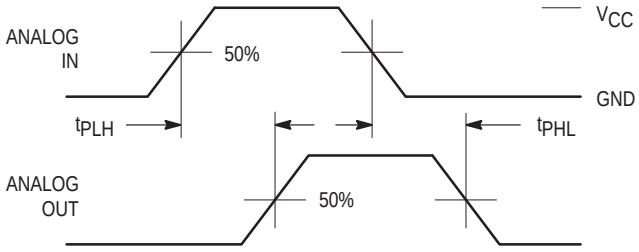
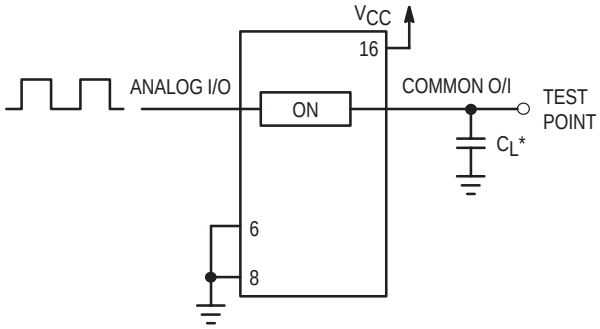


Figure 10a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 10b. Propagation Delay, Test Set–Up Analog In to Analog Out

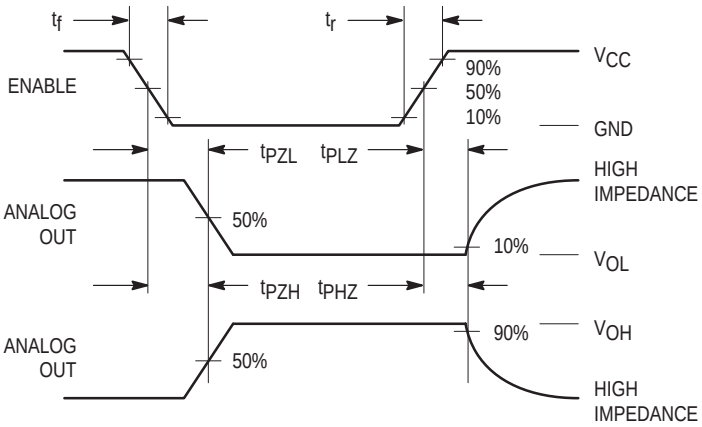


Figure 11a. Propagation Delays, Enable to Analog Out

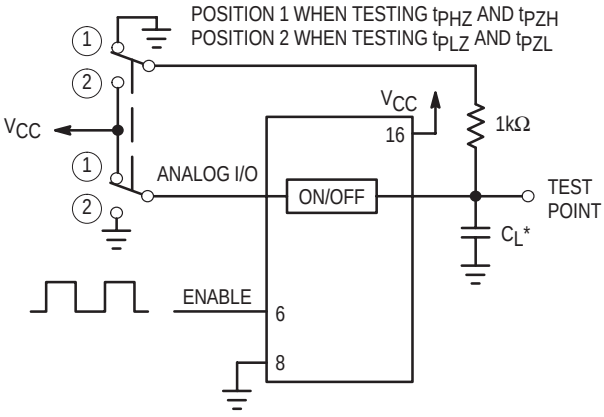


Figure 11b. Propagation Delay, Test Set–Up Enable to Analog Out

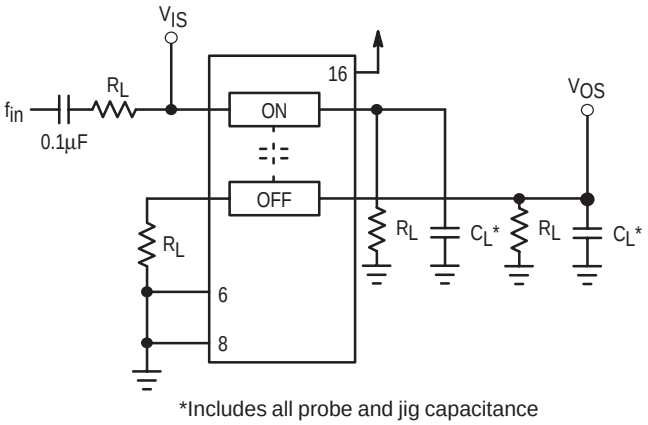


Figure 12. Crosstalk Between Any Two Switches, Test Set–Up

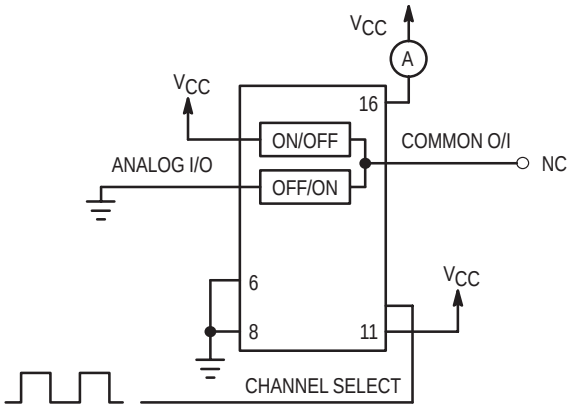


Figure 13. Power Dissipation Capacitance, Test Set–Up

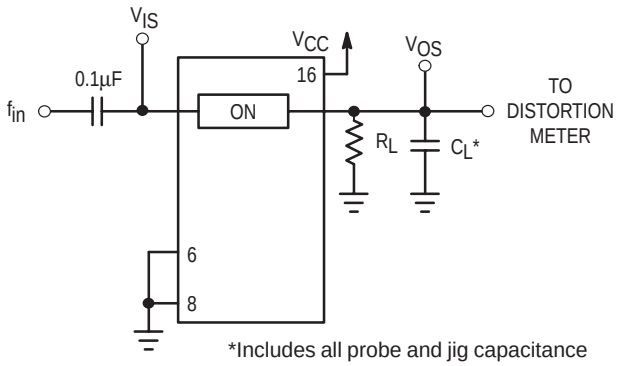


Figure 14a. Total Harmonic Distortion, Test Set–Up

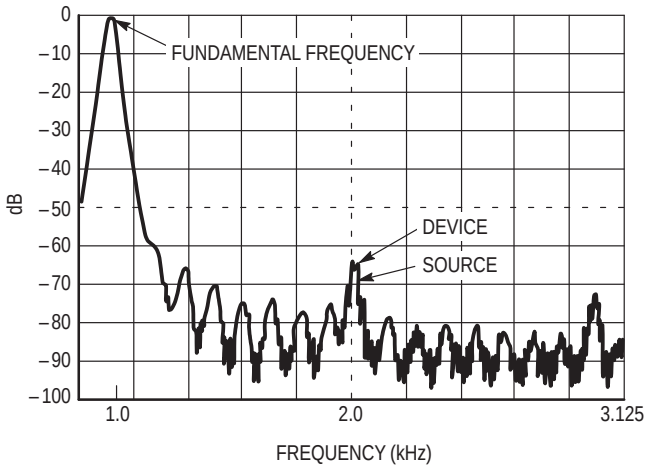


Figure 14b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

V_{CC} = +5V = logic high
GND = 0V = logic low

The maximum analog voltage swing is determined by the supply voltage V_{CC}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below GND. In this example, the difference between V_{CC} and GND is five volts. Therefore, using the configuration of Figure 15, a maximum analog signal of five volts peak–to–peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

V_{CC} – GND = 2 to 6 volts

When voltage transients above V_{CC} and/or below GND are anticipated on the analog channels, external Germanium or Schottky diodes (D_X) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

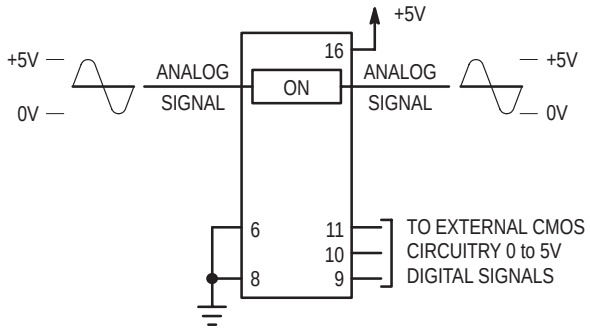


Figure 15. Application Example

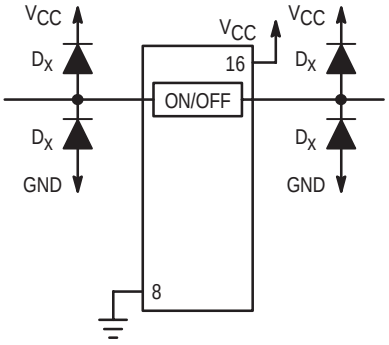
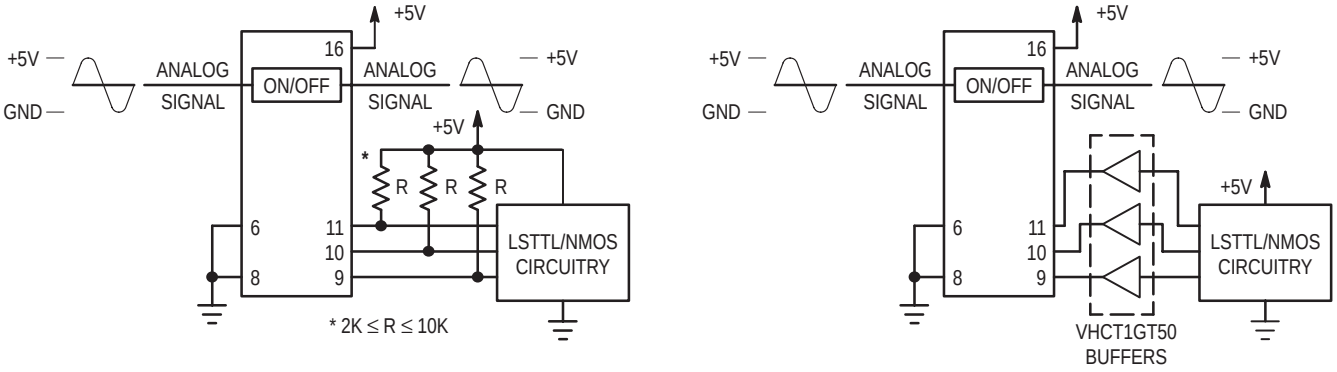


Figure 16. External Germanium or Schottky Clipping Diodes



a. Using Pull–Up Resistors

b. Using HCT Interface

Figure 17. Interfacing LSTTL/NMOS to CMOS Inputs

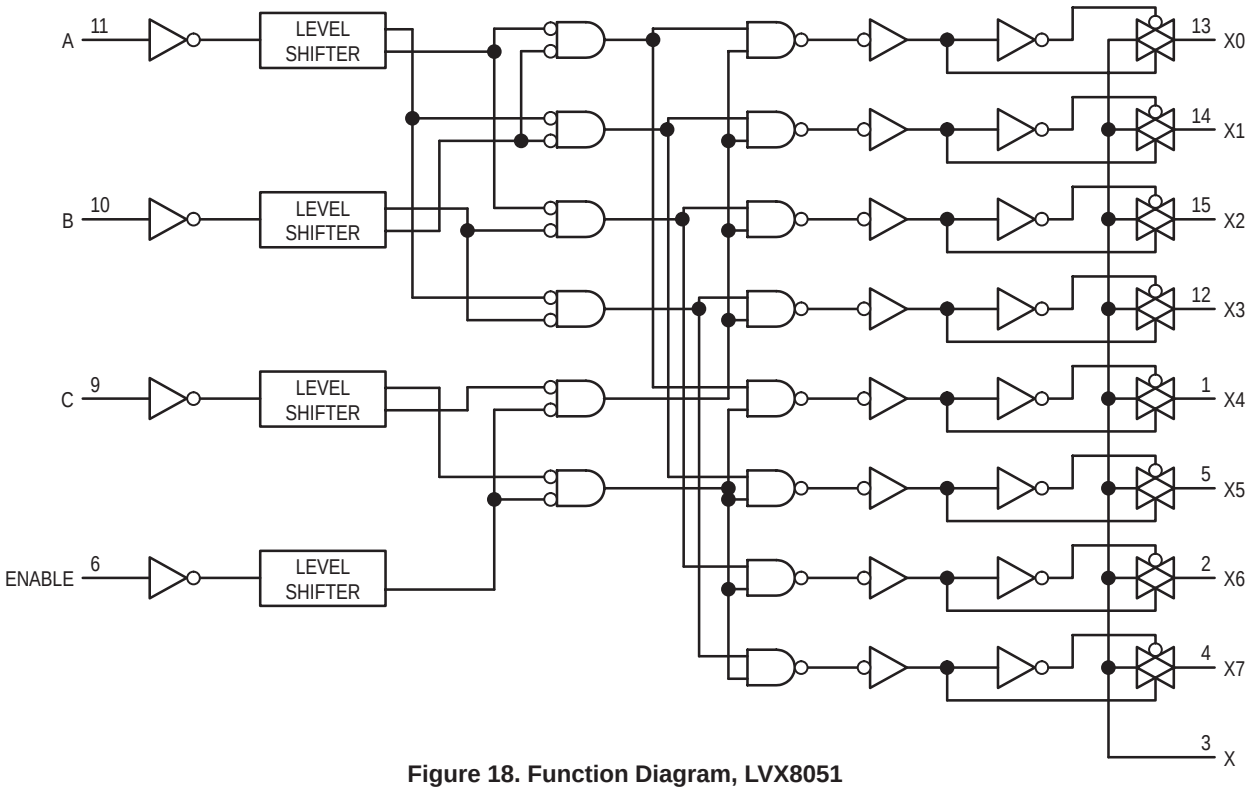
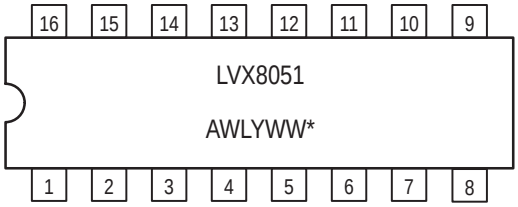
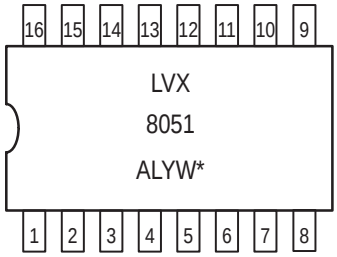


Figure 18. Function Diagram, LVX8051

MARKING DIAGRAMS
(Top View)



16–LEAD SOIC
D SUFFIX
CASE 751B



16–LEAD TSSOP
DT SUFFIX
CASE 948F

*See Applications Note #AND8004/D for date code and traceability information.

MC74LVXT8051

Analog Multiplexer / Demultiplexer

High–Performance Silicon–Gate CMOS

The MC74LVXT8051 utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to GND).

The LVXT8051 is similar in pinout to the high–speed HC4051A and the metal–gate MC14051B. The Channel–Select inputs determine which one of the Analog Inputs/Outputs is to be connected by means of an analog switch to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

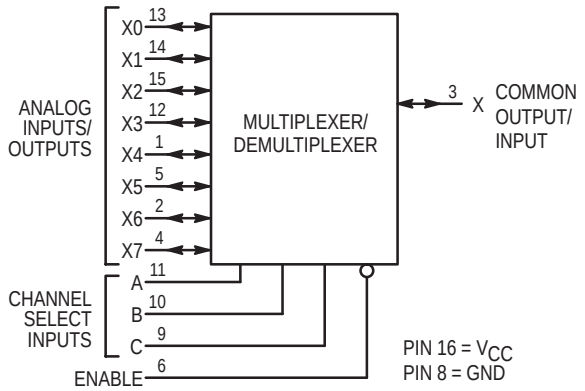
The Channel–Select and Enable inputs are compatible with TTL–type input thresholds. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic–level translator from 3.0V CMOS logic to 5.0V CMOS Logic or from 1.8V CMOS logic to 3.0V CMOS Logic while operating at the higher–voltage power supply.

The MC74LVXT8051 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74LVXT8051 to be used to interface 5V circuits to 3V circuits.

This device has been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal–gate CMOS analog switches.

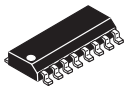
- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Digital (Control) Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal–Gate Counterparts
- Low Noise
- In Compliance With the Requirements of JEDEC Standard No. 7A

LOGIC DIAGRAM
MC74LVXT8051
Single–Pole, 8–Position Plus Common Off

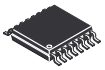


ON Semiconductor

http://onsemi.com

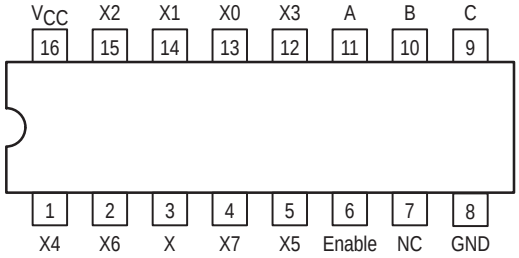


16–LEAD SOIC
D SUFFIX
CASE 751B



16–LEAD TSSOP
DT SUFFIX
CASE 948F

PIN CONNECTION AND MARKING DIAGRAM (Top View)



For detailed package marking information, see the Marking Diagram section on page 172 of this data sheet.

FUNCTION TABLE – MC74LVXT8051

Control Inputs				
	Select			
Enable	C	B	A	ON Channels
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

X = Don't Care

ORDERING INFORMATION

Device	Package	Shipping
MC74LVXT8051D	SOIC	48 Units/Rail
MC74LVXT8051DR2	SOIC	2500 Units/Reel
MC74LVXT8051DT	TSSOP	96 Units/Rail
MC74LVXT8051DTR2	TSSOP	2500 Units/Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{IS}	Analog Input Voltage	– 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin	–20	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IS}	Analog Input Voltage	0.0	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		1.2	V
T_A	Operating Temperature Range, All Package Types	– 55	+ 85	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs) V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	 0 0	 100 20	ns/V

*For voltage drops across switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	3.0 4.5 5.5	1.2 2.0 2.0	1.2 2.0 2.0	1.2 2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	3.0 4.5 5.5	0.53 0.8 0.8	0.53 0.8 0.8	0.53 0.8 0.8	V
I_{in}	Maximum Input Leakage Current, Channel–Select or Enable Inputs	V_{in} = V_{CC} or GND	5.5	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and V_{IS} = V_{CC} or GND; V_{IO} = 0 V	5.5	4	40	160	μA

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
R_{on}	Maximum “ON” Resistance	V_{in} = V_{IL} or V_{IH} V_{IS} = V_{CC} to GND $\|I_S\|$ ≤ 10.0 mA (Figures 1, 2)	3.0 4.5 5.5	40 30 25	45 32 28	50 37 30	Ω
		V_{in} = V_{IL} or V_{IH} V_{IS} = V_{CC} or GND (Endpoints) $\|I_S\|$ ≤ 10.0 mA (Figures 1, 2)	3.0 4.5 5.5	30 25 20	35 28 25	40 35 30	
ΔR_{on}	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	V_{in} = V_{IL} or V_{IH} V_{IS} = 1/2 (V_{CC} – GND) $\|I_S\|$ ≤ 10.0 mA	3.0 4.5 5.5	15 8.0 8.0	20 12 12	25 15 15	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} or GND; Switch Off (Figure 3)	5.5	0.1	0.5	1.0	μA
	Maximum Off–Channel Leakage Current, Common Channel	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} or GND; Switch Off (Figure 4)	5.5	0.2	2.0	4.0	
I_{on}	Maximum On–Channel Leakage Current, Channel–to–Channel	V_{in} = V_{IL} or V_{IH}; Switch–to–Switch = V_{CC} or GND; (Figure 5)	5.5	0.2	2.0	4.0	μA

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 3 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Channel–Select to Analog Output (Figure 9)	2.0 3.0 4.5 5.5	30 20 15 15	35 25 18 18	40 30 22 20	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0 3.0 4.5 5.5	4.0 3.0 1.0 1.0	6.0 5.0 2.0 2.0	8.0 6.0 2.0 2.0	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 5.5	30 20 15 15	35 25 18 18	40 30 22 20	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 5.5	20 12 8.0 8.0	25 14 10 10	30 15 12 12	ns
C_{in}	Maximum Input Capacitance, Channel–Select or Enable Inputs		10	10	10	pF
$C_{I/O}$	Maximum Capacitance — Analog I/O		35	35	35	pF
	(All Switches Off) — Common O/I		130	130	130	
	Feedthrough		1.0	1.0	1.0	

C_{PD}		**Typical @ 25°C, V_{CC} = 5.0 V**	pF
	Power Dissipation Capacitance (Figure 13)*	45	

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V_{CC} V	Limit* 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 6)	f_{in} = 1MHz Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{OS}; Increase f_{in} Frequency Until dB Meter Reads –3dB; R_L = 50Ω, C_L = 10pF	3.0 4.5 5.5	80 80 80	MHz
—	Off–Channel Feedthrough Isolation (Figure 7)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600Ω, C_L = 50pF	3.0 4.5 5.5	–50 –50 –50	dB
		f_{in} = 1.0MHz, R_L = 50Ω, C_L = 10pF	3.0 4.5 5.5	–37 –37 –37	
—	Feedthrough Noise. Channel–Select Input to Common I/O (Figure 8)	$V_{in} \leq$ 1MHz Square Wave ($t_r = t_f$ = 3ns); Adjust R_L at Setup so that I_S = 0A; Enable = GND R_L = 600Ω, C_L = 50pF	3.0 4.5 5.5	25 105 135	mV_{PP}
		R_L = 10kΩ, C_L = 10pF	3.0 4.5 5.5	35 145 190	
—	Crosstalk Between Any Two Switches (Figure 12)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600Ω, C_L = 50pF	3.0 4.5 5.5	–50 –50 –50	dB
		f_{in} = 1.0MHz, R_L = 50Ω, C_L = 10pF	3.0 4.5 5.5	–60 –60 –60	
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1kHz, R_L = 10kΩ, C_L = 50pF $THD = THD_{measured} - THD_{source}$ V_{IS} = 2.0V_{PP} sine wave V_{IS} = 4.0V_{PP} sine wave V_{IS} = 5.0V_{PP} sine wave	 3.0 4.5 5.5	 0.10 0.08 0.05	%

*Limits not tested. Determined by design and verified by qualification.

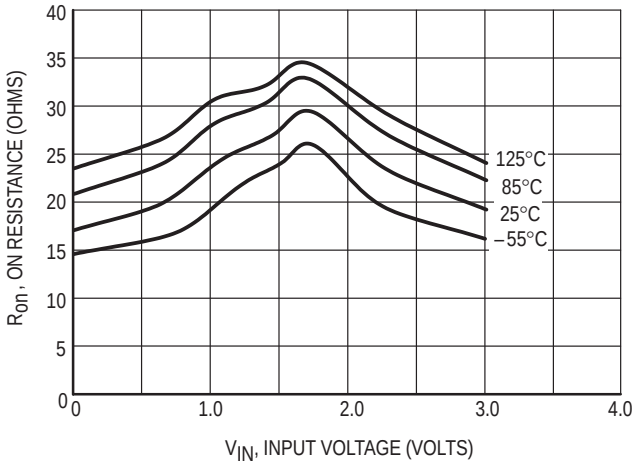


Figure 1a. Typical On Resistance, V_{CC} = 3.0 V

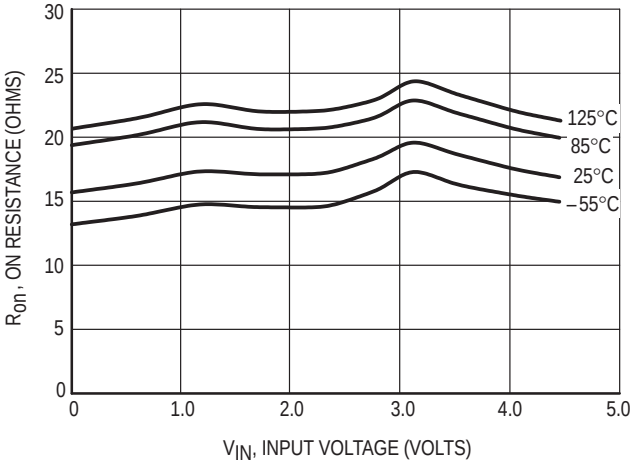


Figure 1b. Typical On Resistance, V_{CC} = 4.5 V

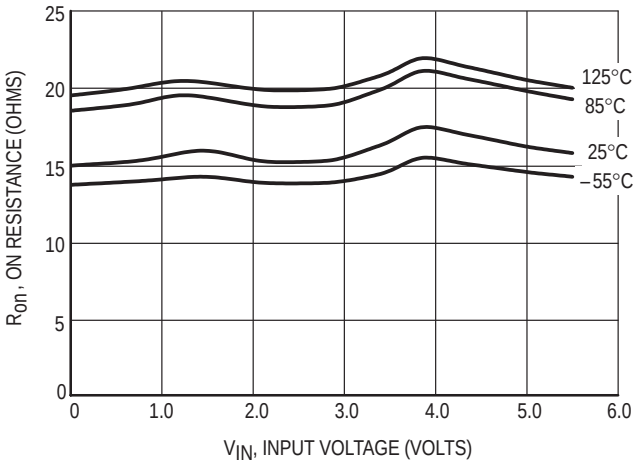


Figure 1c. Typical On Resistance, V_{CC} = 5.5 V

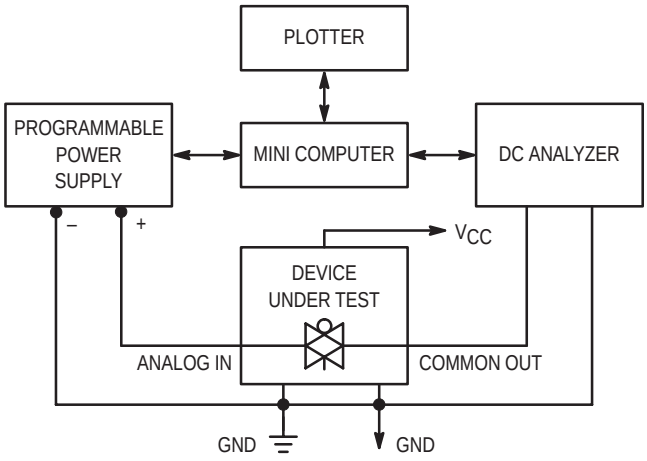


Figure 2. On Resistance Test Set–Up

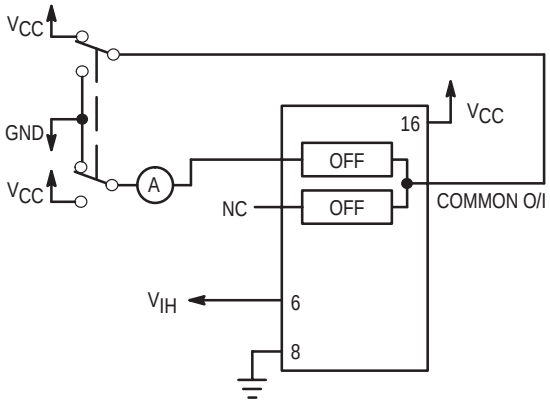


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

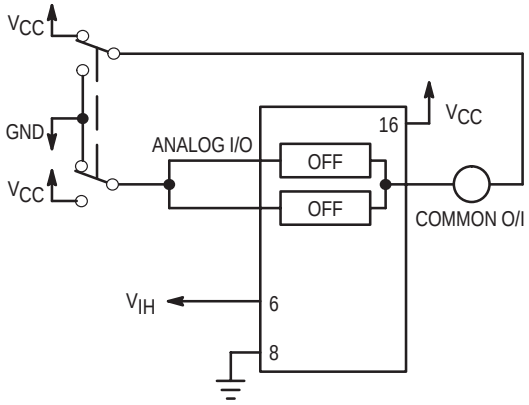


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set–Up

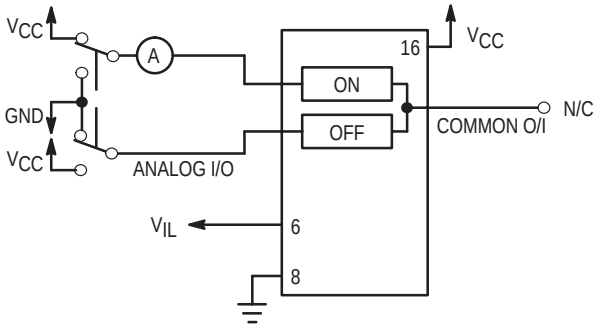
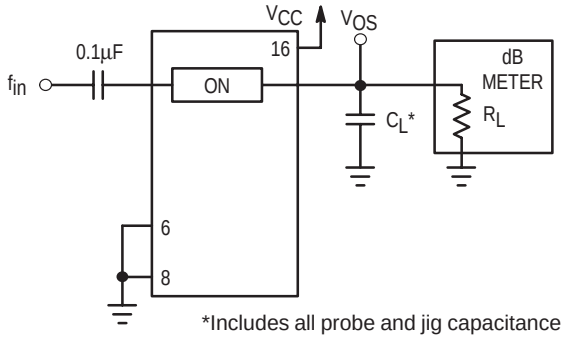
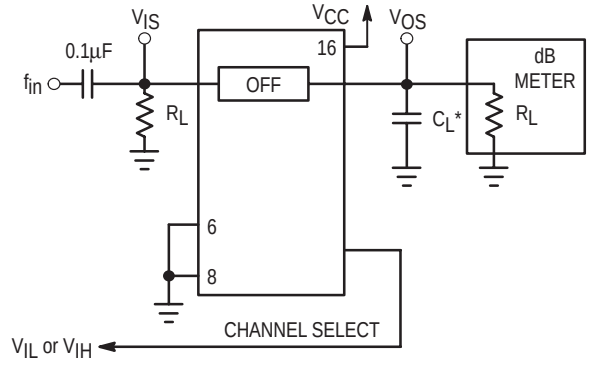


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set–Up



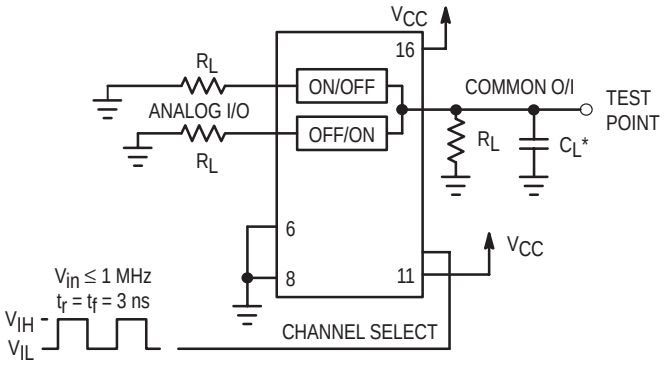
*Includes all probe and jig capacitance

Figure 6. Maximum On Channel Bandwidth, Test Set–Up



*Includes all probe and jig capacitance

Figure 7. Off Channel Feedthrough Isolation, Test Set–Up



*Includes all probe and jig capacitance

Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set–Up

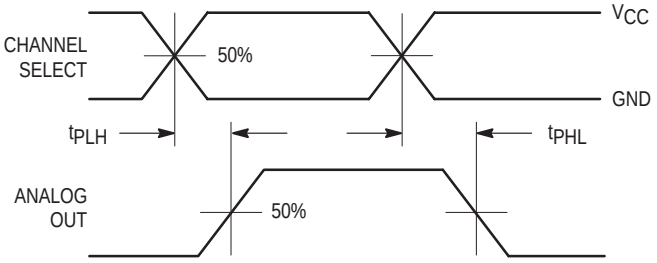
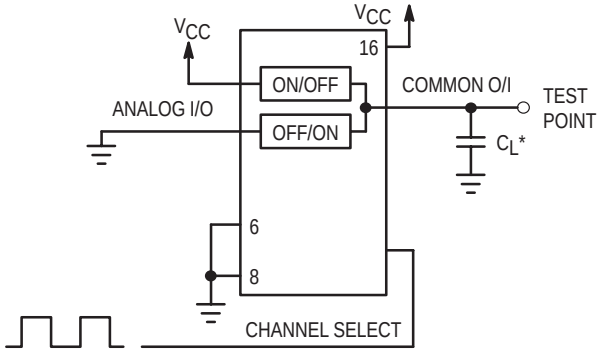


Figure 9a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 9b. Propagation Delay, Test Set–Up Channel Select to Analog Out

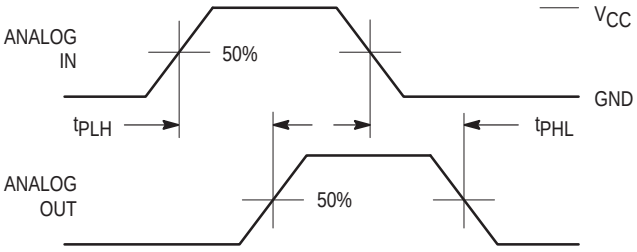
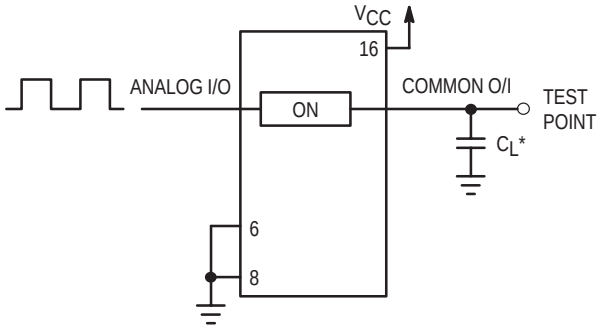


Figure 10a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 10b. Propagation Delay, Test Set–Up Analog In to Analog Out

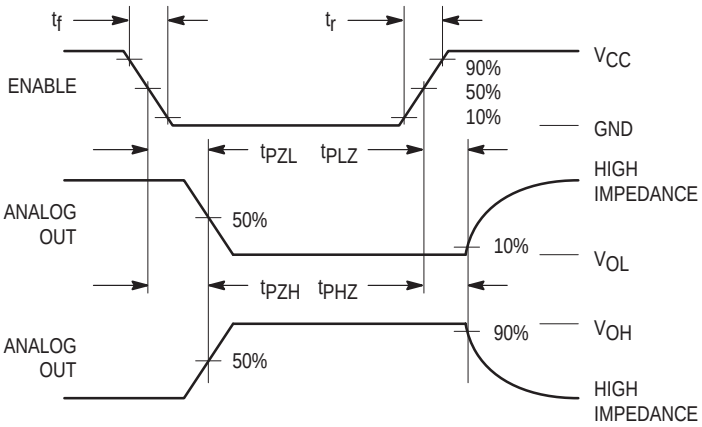


Figure 11a. Propagation Delays, Enable to Analog Out

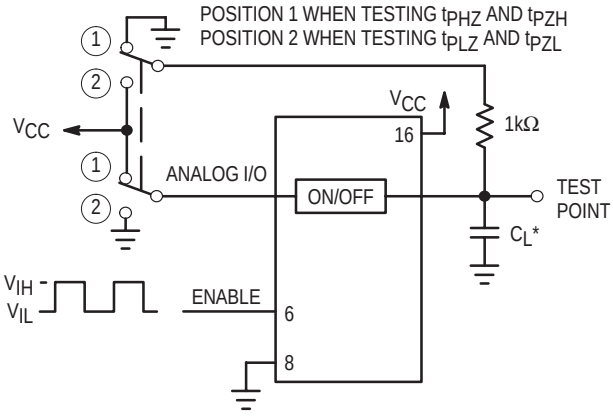


Figure 11b. Propagation Delay, Test Set–Up Enable to Analog Out

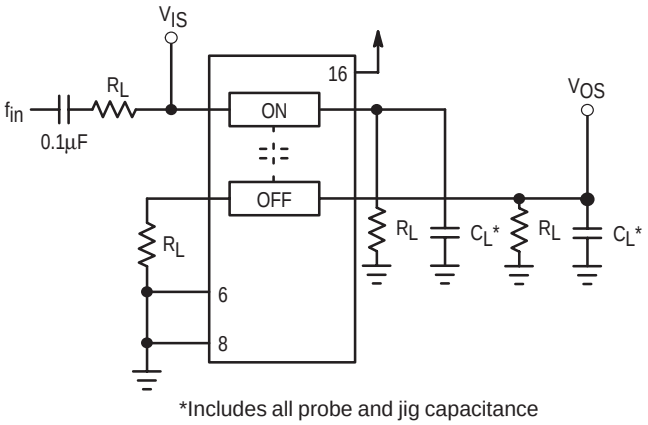


Figure 12. Crosstalk Between Any Two Switches, Test Set–Up

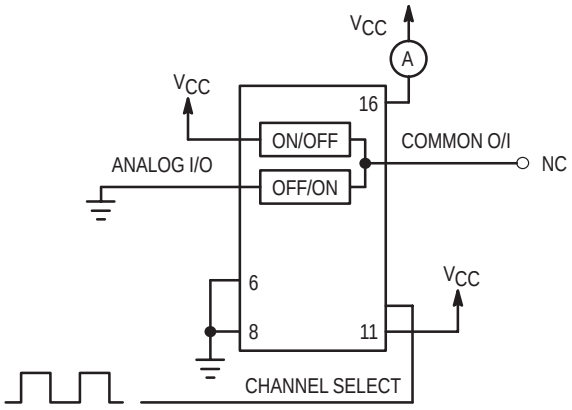


Figure 13. Power Dissipation Capacitance, Test Set–Up

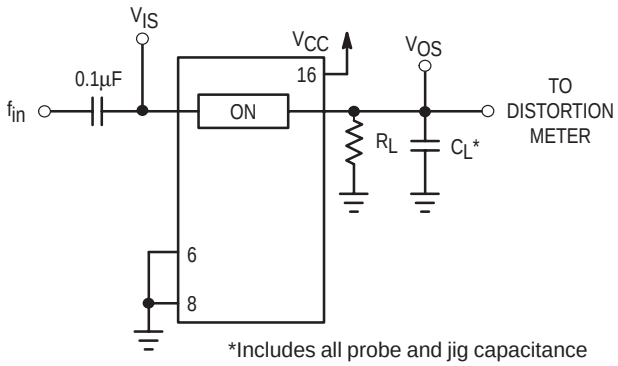


Figure 14a. Total Harmonic Distortion, Test Set–Up

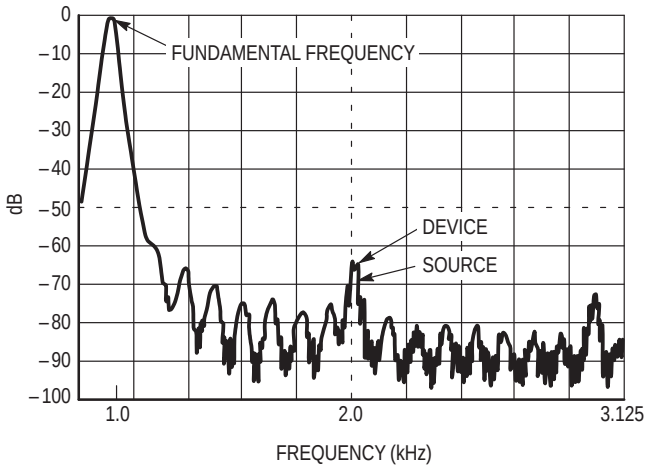


Figure 14b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

V_{CC} = +5V = logic high
GND = 0V = logic low

The maximum analog voltage swing is determined by the supply voltage V_{CC}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below GND. In this example, the difference between V_{CC} and GND is five volts. Therefore, using the configuration of Figure 15, a maximum analog signal of five volts peak–to–peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

V_{CC} – GND = 2 to 6 volts

When voltage transients above V_{CC} and/or below GND are anticipated on the analog channels, external Germanium or Schottky diodes (D_X) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

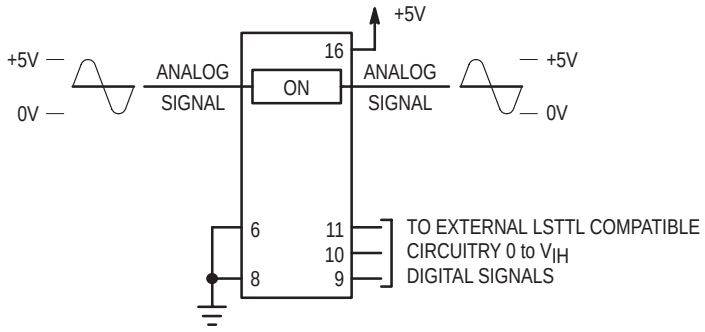


Figure 15. Application Example

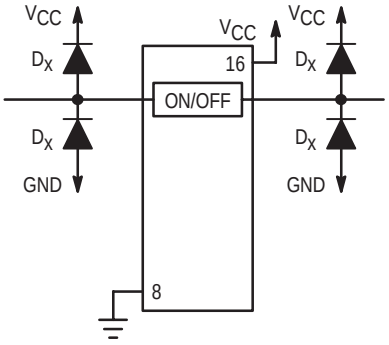
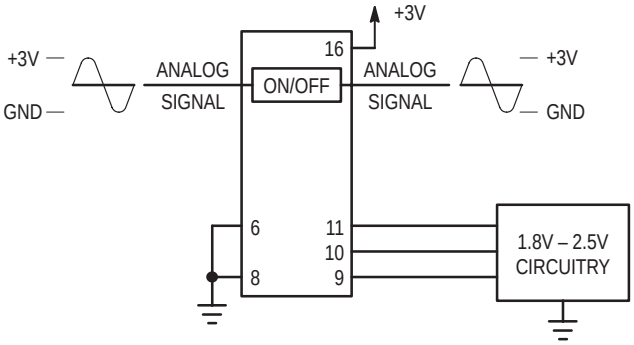
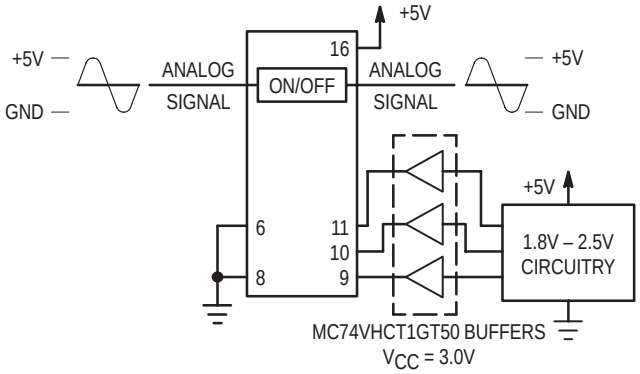


Figure 16. External Germanium or Schottky Clipping Diodes



a. Low Voltage Logic Level Shifting Control



b. 2–Stage Logic Level Shifting Control

Figure 17. Interfacing to Low Voltage CMOS Outputs

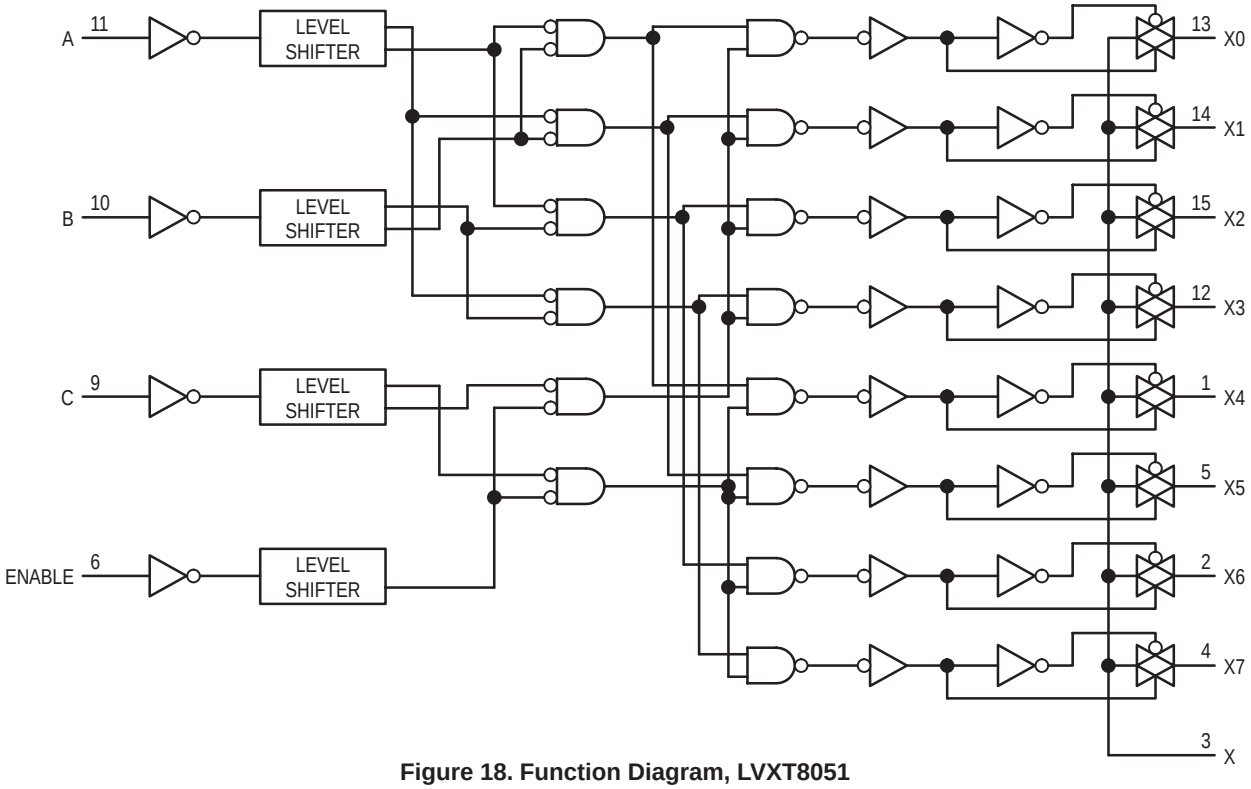
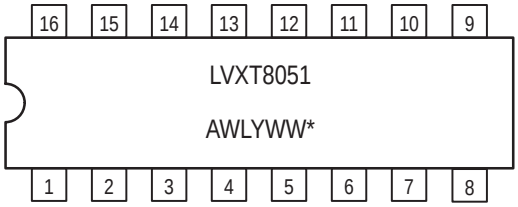
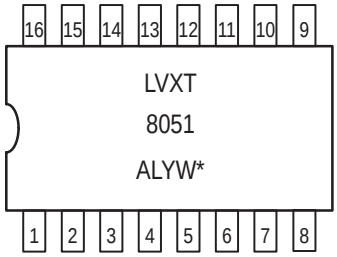


Figure 18. Function Diagram, LVXT8051

MARKING DIAGRAMS
(Top View)



16–LEAD SOIC
D SUFFIX
CASE 751B



16–LEAD TSSOP
DT SUFFIX
CASE 948F

*See Applications Note #AND8004/D for date code and traceability information.

MC74LVX8053

Analog Multiplexer / Demultiplexer

High–Performance Silicon–Gate CMOS

The MC74LVX8053 utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to GND).

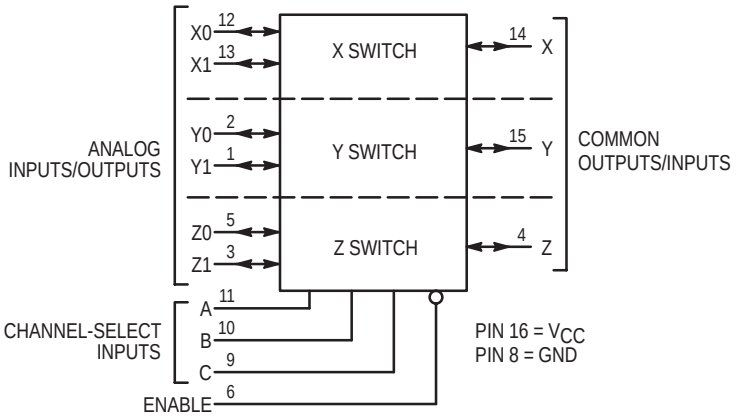
The LVX8053 is similar in pinout to the high–speed HC4053A, and the metal–gate MC14053B. The Channel–Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel–Select and Enable inputs are compatible with standard CMOS outputs; with pull–up resistors they are compatible with LSTTL outputs.

This device has been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal–gate CMOS analog switches.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Digital (Control) Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal–Gate Counterparts
- Low Noise
- In Compliance With the Requirements of JEDEC Standard No. 7A
- Chip Complexity: LVX8053 — 156 FETs or 39 Equivalent Gates

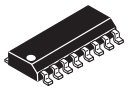
LOGIC DIAGRAM
Triple Single–Pole, Double–Position Plus Common Off



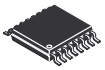
NOTE: This device allows independent control of each switch. Channel–Select Input A controls the X–Switch, Input B controls the Y–Switch and Input C controls the Z–Switch

ON Semiconductor

http://onsemi.com

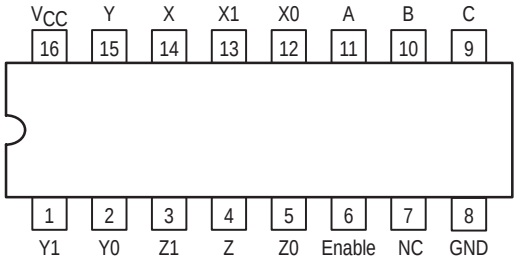


16–LEAD SOIC
D SUFFIX
CASE 751B



16–LEAD TSSOP
DT SUFFIX
CASE 948F

PIN CONNECTION AND MARKING DIAGRAM (Top View)



For detailed package marking information, see the Marking Diagram section on page 183 of this data sheet.

FUNCTION TABLE – MC74LVX8053

Control Inputs						
Enable	Select C	Select B	Select A	ON Channels		
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	NONE		

X = Don't Care

ORDERING INFORMATION

Device	Package	Shipping
MC74LVX8053D	SOIC	48 Units/Rail
MC74LVX8053DR2	SOIC	2500 Units/Reel
MC74LVX8053DT	TSSOP	96 Units/Rail
MC74LVX8053DTR2	TSSOP	2500 Units/Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{IS}	Analog Input Voltage	– 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin	± 20	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IS}	Analog Input Voltage	0.0	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		1.2	V
T_A	Operating Temperature Range, All Package Types	– 55	+ 85	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs) V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	 0 0	 100 20	ns/V

*For voltage drops across switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 5.5	1.50 2.10 3.15 3.85	1.50 2.10 3.15 3.85	1.50 2.10 3.15 3.85	V
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 5.5	0.5 0.9 1.35 1.65	0.5 0.9 1.35 1.65	0.5 0.9 1.35 1.65	V
I_{in}	Maximum Input Leakage Current, Channel–Select or Enable Inputs	V_{in} = V_{CC} or GND,	5.5	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and V_{IS} = V_{CC} or GND; V_{IO} = 0 V	5.5	4	40	160	μA

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
R_{on}	Maximum “ON” Resistance	V_{in} = V_{IL} or V_{IH} V_{IS} = V_{CC} to GND $\|I_S\|$ ≤ 10.0 mA (Figures 1, 2)	3.0 4.5 5.5	40 30 25	45 32 28	50 37 30	Ω
		V_{in} = V_{IL} or V_{IH} V_{IS} = V_{CC} or GND (Endpoints) $\|I_S\|$ ≤ 10.0 mA (Figures 1, 2)	3.0 4.5 5.5	30 25 20	35 28 25	40 35 30	
ΔR_{on}	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	V_{in} = V_{IL} or V_{IH} V_{IS} = 1/2 (V_{CC} – GND) $\|I_S\|$ ≤ 10.0 mA	3.0 4.5 5.5	15 8.0 8.0	20 12 12	25 15 15	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} or GND; Switch Off (Figure 3)	5.5	0.1	0.5	1.0	μA
	Maximum Off–Channel Leakage Current, Common Channel	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} or GND; Switch Off (Figure 4)	5.5	0.1	1.0	2.0	
I_{on}	Maximum On–Channel Leakage Current, Channel–to–Channel	V_{in} = V_{IL} or V_{IH}; Switch–to–Switch = V_{CC} or GND; (Figure 5)	5.5	0.1	1.0	2.0	μA

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 3 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Channel–Select to Analog Output (Figure 9)	2.0 3.0 4.5 5.5	30 20 15 15	35 25 18 18	40 30 22 20	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0 3.0 4.5 5.5	4.0 3.0 1.0 1.0	6.0 5.0 2.0 2.0	8.0 6.0 2.0 2.0	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 5.5	30 20 15 15	35 25 18 18	40 30 22 20	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 5.5	20 12 8.0 8.0	25 14 10 10	30 15 12 12	ns
C_{in}	Maximum Input Capacitance, Channel–Select or Enable Inputs		10	10	10	pF
$C_{I/O}$	Maximum Capacitance (All Switches Off) — Analog I/O		35	35	35	pF
	Common O/I		50	50	50	
	Feedthrough		1.0	1.0	1.0	

C_{PD}		**Typical @ 25°C, V_{CC} = 5.0 V**	pF
	Power Dissipation Capacitance (Figure 13)*	45	

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V_{CC} V	Limit* 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 6)	f_{in} = 1MHz Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{OS}; Increase f_{in} Frequency Until dB Meter Reads –3dB; R_L = 50Ω, C_L = 10pF	3.0 4.5 5.5	 120 120 120	MHz
—	Off–Channel Feedthrough Isolation (Figure 7)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600Ω, C_L = 50pF	3.0 4.5 5.5	–50 –50 –50	dB
		f_{in} = 1.0MHz, R_L = 50Ω, C_L = 10pF	3.0 4.5 5.5	–37 –37 –37	
—	Feedthrough Noise. Channel–Select Input to Common I/O (Figure 8)	$V_{in} \leq$ 1MHz Square Wave ($t_r = t_f$ = 6ns); Adjust R_L at Setup so that I_S = 0A; Enable = GND R_L = 600Ω, C_L = 50pF	3.0 4.5 5.5	25 105 135	mV_{PP}
		R_L = 10kΩ, C_L = 10pF	3.0 4.5 5.5	35 145 190	
—	Crosstalk Between Any Two Switches (Figure 12)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600Ω, C_L = 50pF	3.0 4.5 5.5	–50 –50 –50	dB
		f_{in} = 1.0MHz, R_L = 50Ω, C_L = 10pF	3.0 4.5 5.5	–60 –60 –60	
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1kHz, R_L = 10kΩ, C_L = 50pF $THD = THD_{measured} - THD_{source}$ V_{IS} = 2.0V_{PP} sine wave V_{IS} = 4.0V_{PP} sine wave V_{IS} = 5.5V_{PP} sine wave	 3.0 4.5 5.5	 0.10 0.08 0.05	%

*Limits not tested. Determined by design and verified by qualification.

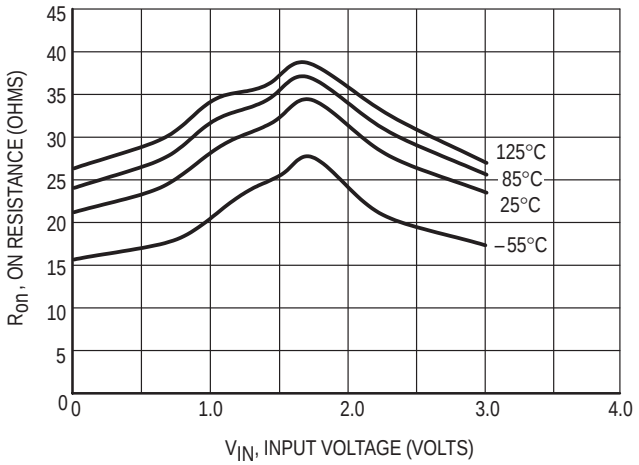


Figure 1a. Typical On Resistance, V_{CC} = 3.0 V

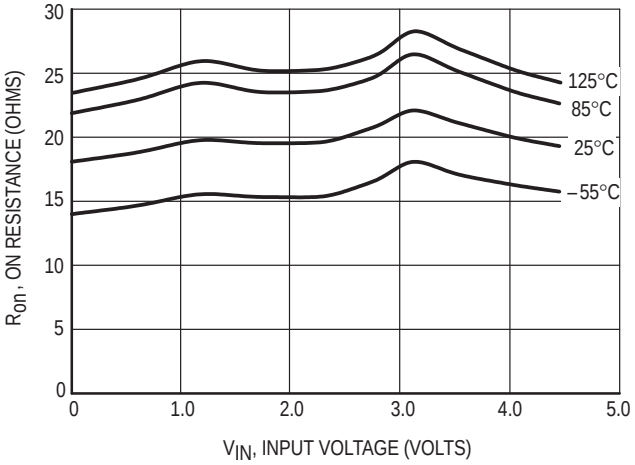


Figure 1b. Typical On Resistance, V_{CC} = 4.5 V

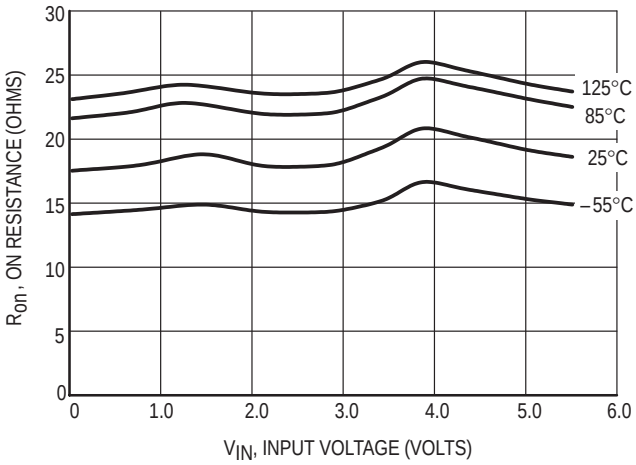


Figure 1c. Typical On Resistance, V_{CC} = 5.5 V

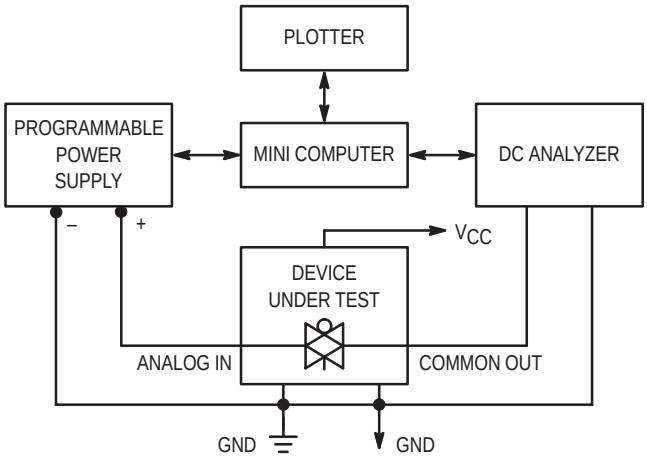


Figure 2. On Resistance Test Set–Up

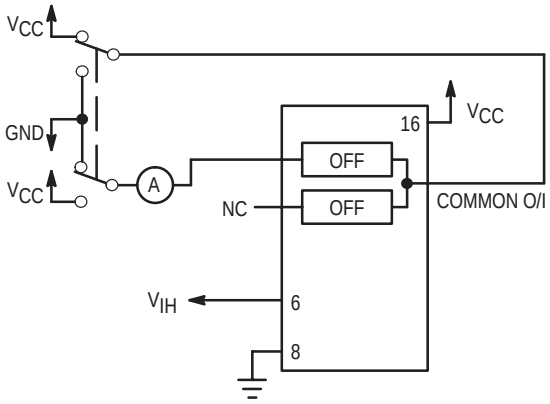


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

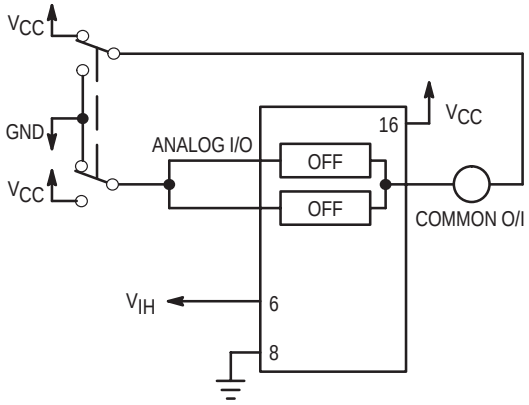


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set–Up

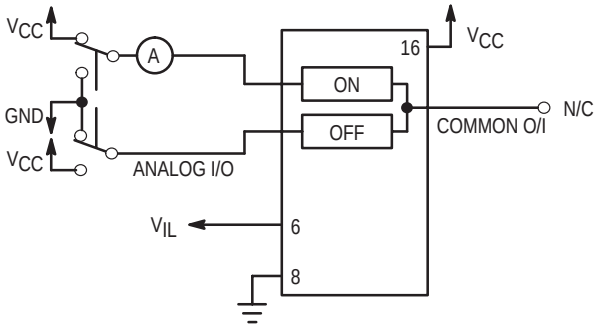
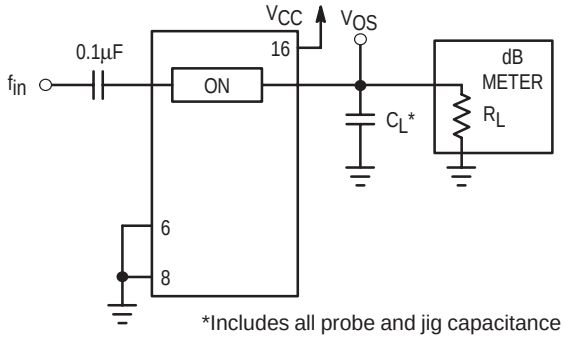
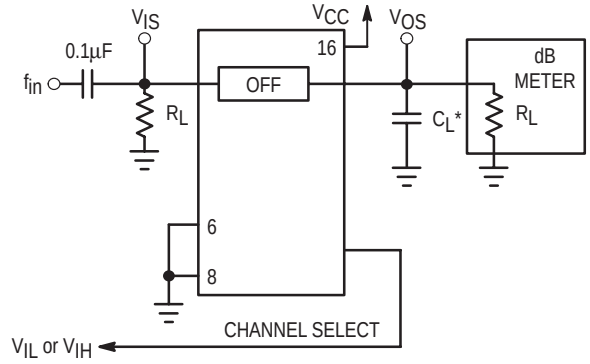


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set–Up



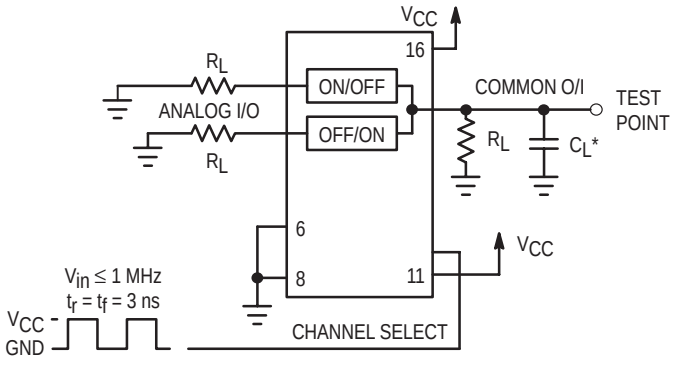
*Includes all probe and jig capacitance

Figure 6. Maximum On Channel Bandwidth, Test Set–Up



*Includes all probe and jig capacitance

Figure 7. Off Channel Feedthrough Isolation, Test Set–Up



*Includes all probe and jig capacitance

Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set–Up

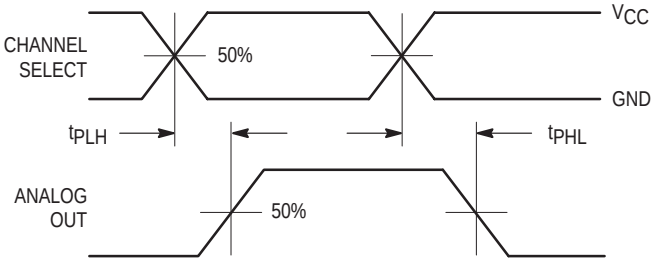
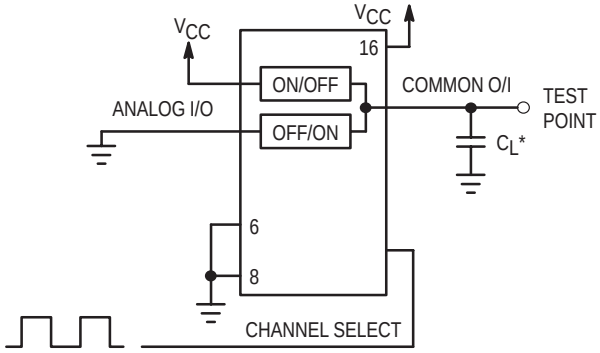


Figure 9a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 9b. Propagation Delay, Test Set–Up Channel Select to Analog Out

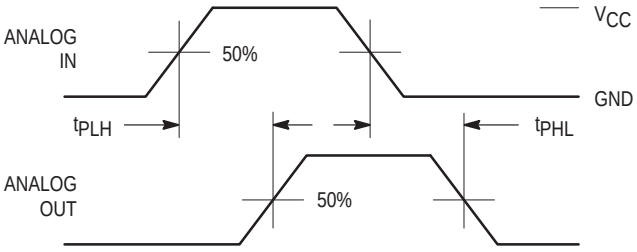
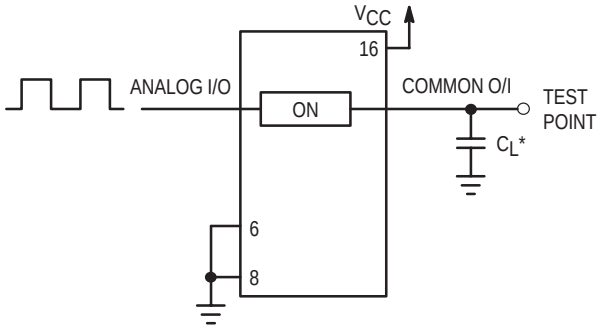


Figure 10a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 10b. Propagation Delay, Test Set–Up Analog In to Analog Out

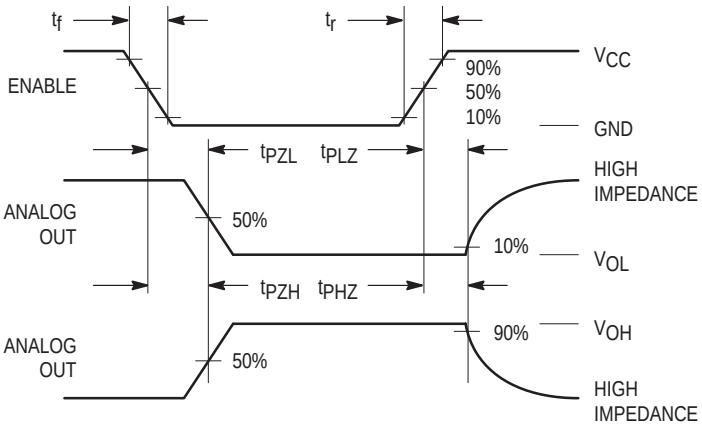


Figure 11a. Propagation Delays, Enable to Analog Out

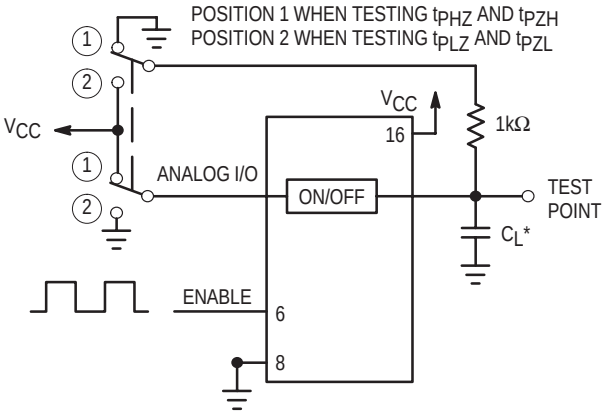


Figure 11b. Propagation Delay, Test Set–Up Enable to Analog Out

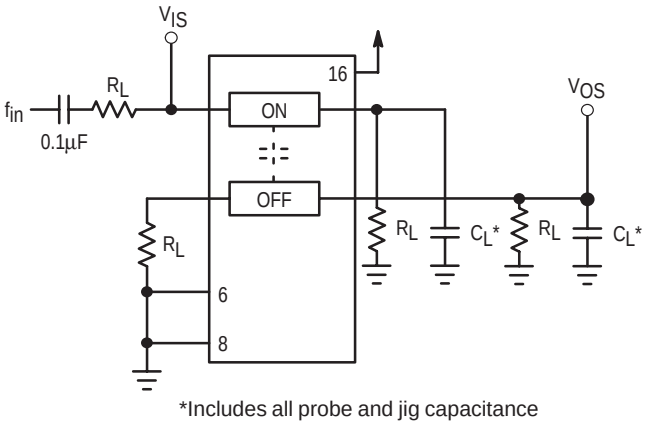


Figure 12. Crosstalk Between Any Two Switches, Test Set–Up

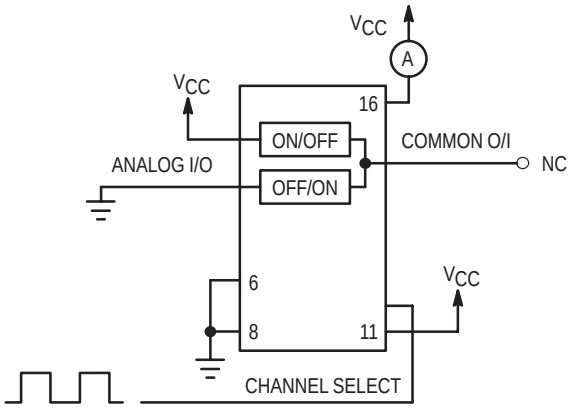


Figure 13. Power Dissipation Capacitance, Test Set–Up

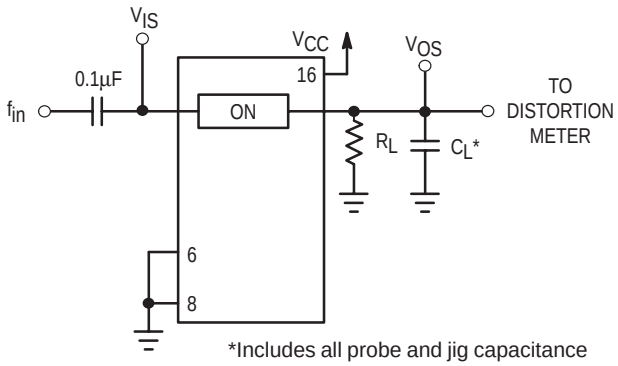


Figure 14a. Total Harmonic Distortion, Test Set–Up

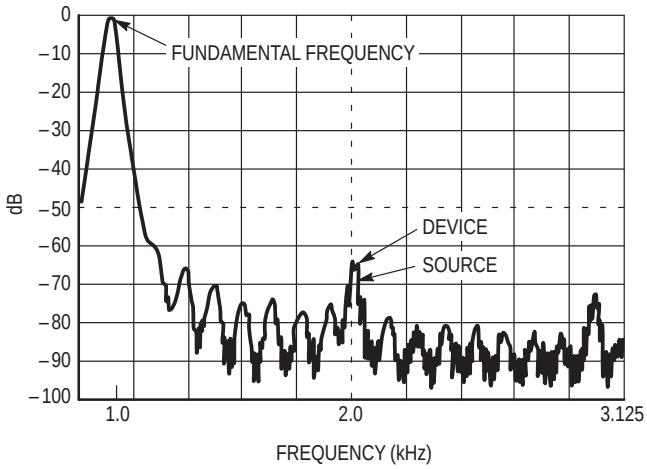


Figure 14b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

V_{CC} = +5V = logic high
GND = 0V = logic low

The maximum analog voltage swing is determined by the supply voltages V_{CC}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below GND. In this example, the difference between V_{CC} and GND is five volts. Therefore, using the configuration of Figure 15, a maximum analog signal of five volts peak–to–peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

V_{CC} – GND = 2 to 6 volts

When voltage transients above V_{CC} and/or below GND are anticipated on the analog channels, external Germanium or Schottky diodes (D_X) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

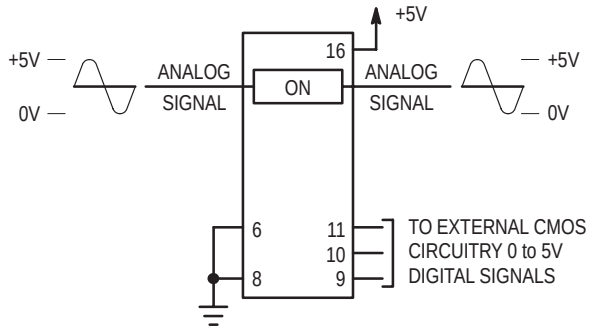


Figure 15. Application Example

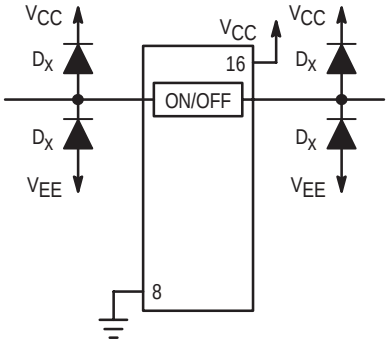
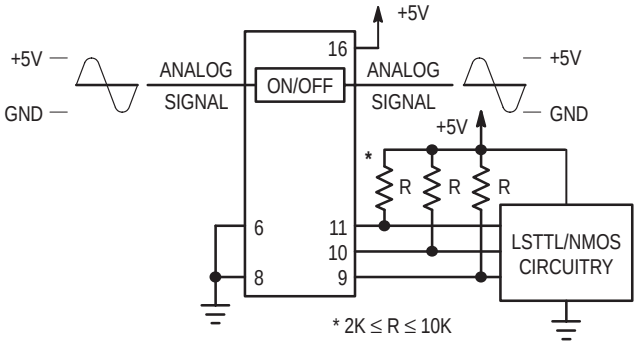
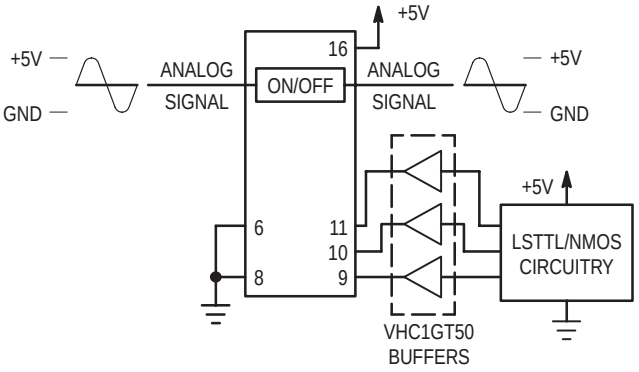


Figure 16. External Germanium or Schottky Clipping Diodes



a. Using Pull–Up Resistors



b. Using HCT Interface

Figure 17. Interfacing LSTTL/NMOS to CMOS Inputs

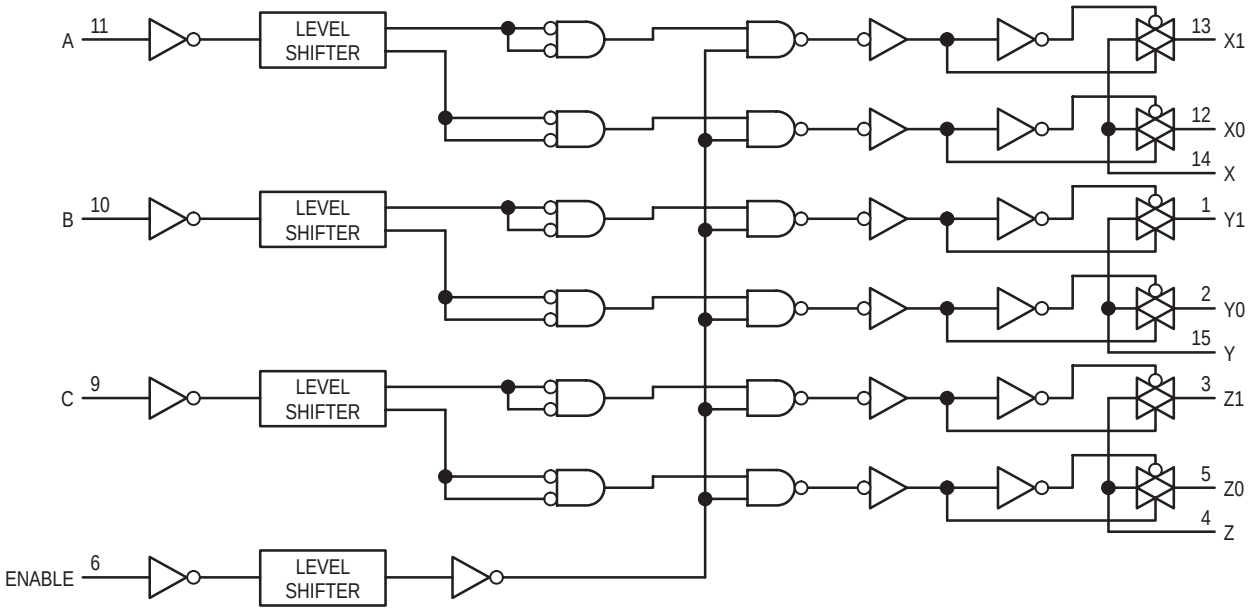
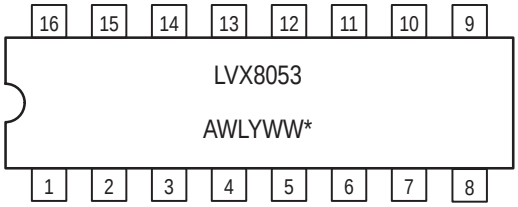
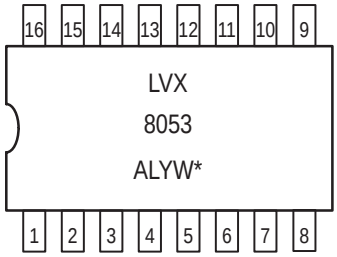


Figure 18. Function Diagram, LVX8053

MARKING DIAGRAMS
(Top View)



16–LEAD SOIC
D SUFFIX
CASE 751B



16–LEAD TSSOP
DT SUFFIX
CASE 948F

*See Applications Note #AND8004/D for date code and traceability information.

MC74LVXT8053

Analog Multiplexer / Demultiplexer

High–Performance Silicon–Gate CMOS

The MC74LVXT8053 utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to GND).

The LVXT8053 is similar in pinout to the high–speed HC4053A, and the metal–gate MC14053B. The Channel–Select inputs determine which one of the Analog Inputs/Outputs is to be connected by means of an analog switch to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel–Select and Enable inputs are compatible with TTL–type input thresholds. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic–level translator from 3.0V CMOS logic to 5.0V CMOS Logic or from 1.8V CMOS logic to 3.0V CMOS Logic while operating at the higher–voltage power supply.

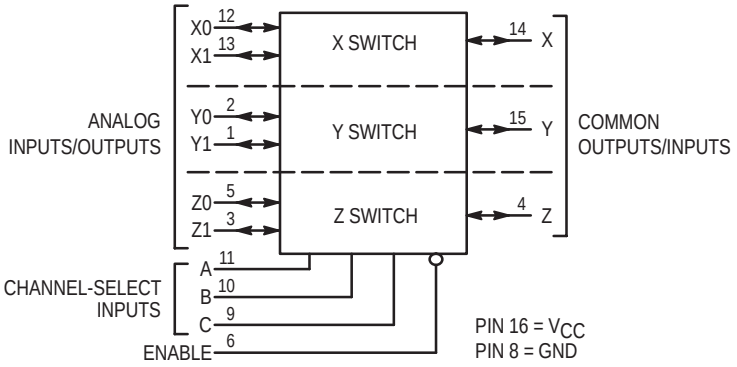
The MC74LVXT8053 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74LVXT8053 to be used to interface 5V circuits to 3V circuits.

This device has been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal–gate CMOS analog switches.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Digital (Control) Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal–Gate Counterparts
- Low Noise
- In Compliance With the Requirements of JEDEC Standard No. 7A

LOGIC DIAGRAM

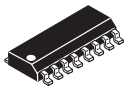
Triple Single–Pole, Double–Position Plus Common Off



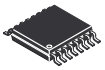
NOTE: This device allows independent control of each switch. Channel–Select Input A controls the X–Switch, Input B controls the Y–Switch and Input C controls the Z–Switch

ON Semiconductor

http://onsemi.com

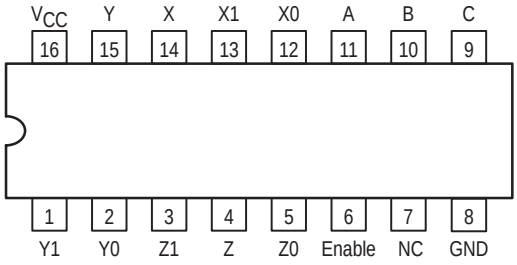


16–LEAD SOIC
D SUFFIX
CASE 751B



16–LEAD TSSOP
DT SUFFIX
CASE 948F

PIN CONNECTION AND MARKING DIAGRAM (Top View)



For detailed package marking information, see the Marking Diagram section on page 194 of this data sheet.

FUNCTION TABLE – MC74LVXT8053

Control Inputs						
	Select					
Enable	C	B	A	ON Channels		
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	NONE		

X = Don't Care

ORDERING INFORMATION

Device	Package	Shipping
MC74LVXT8053D	SOIC	48 Units/Rail
MC74LVXT8053DR2	SOIC	2500 Units/Reel
MC74LVXT8053DT	TSSOP	96 Units/Rail
MC74LVXT8053DTR2	TSSOP	2500 Units/Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{IS}	Analog Input Voltage	– 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin	–20	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IS}	Analog Input Voltage	0.0	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		1.2	V
T_A	Operating Temperature Range, All Package Types	– 55	+ 85	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs) V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	 0 0	 100 20	ns/V

*For voltage drops across switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	3.0 4.5 5.5	1.2 2.0 2.0	1.2 2.0 2.0	1.2 2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	3.0 4.5 5.5	0.53 0.8 0.8	0.53 0.8 0.8	0.53 0.8 0.8	V
I_{in}	Maximum Input Leakage Current, Channel–Select or Enable Inputs	V_{in} = V_{CC} or GND,	5.5	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and V_{IS} = V_{CC} or GND; V_{IO} = 0 V	5.5	4	40	160	μA

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
R_{on}	Maximum “ON” Resistance	V_{in} = V_{IL} or V_{IH} V_{IS} = V_{CC} to GND $\|I_S\|$ ≤ 10.0 mA (Figures 1, 2)	3.0 4.5 5.5	40 30 25	45 32 28	50 37 30	Ω
		V_{in} = V_{IL} or V_{IH} V_{IS} = V_{CC} or GND (Endpoints) $\|I_S\|$ ≤ 10.0 mA (Figures 1, 2)	3.0 4.5 5.5	30 25 20	35 28 25	40 35 30	
ΔR_{on}	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	V_{in} = V_{IL} or V_{IH} V_{IS} = 1/2 (V_{CC} – GND) $\|I_S\|$ ≤ 10.0 mA	3.0 4.5 5.5	15 8.0 8.0	20 12 12	25 15 15	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} or GND; Switch Off (Figure 3)	5.5	0.1	0.5	1.0	μA
	Maximum Off–Channel Leakage Current, Common Channel	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} or GND; Switch Off (Figure 4)	5.5	0.1	1.0	2.0	
I_{on}	Maximum On–Channel Leakage Current, Channel–to–Channel	V_{in} = V_{IL} or V_{IH}; Switch–to–Switch = V_{CC} or GND; (Figure 5)	5.5	0.1	1.0	2.0	μA

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 3 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Channel–Select to Analog Output (Figure 9)	2.0 3.0 4.5 5.5	30 20 15 15	35 25 18 18	40 30 22 20	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0 3.0 4.5 5.5	4.0 3.0 1.0 1.0	6.0 5.0 2.0 2.0	8.0 6.0 2.0 2.0	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 5.5	30 20 15 15	35 25 18 18	40 30 22 20	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 5.5	20 12 8.0 8.0	25 14 10 10	30 15 12 12	ns
C_{in}	Maximum Input Capacitance, Channel–Select or Enable Inputs		10	10	10	pF
$C_{I/O}$	Maximum Capacitance (All Switches Off) — Analog I/O		35	35	35	pF
	Common O/I		50	50	50	
	Feedthrough		1.0	1.0	1.0	

C_{PD}		**Typical @ 25°C, V_{CC} = 5.0 V**	pF
	Power Dissipation Capacitance (Figure 13)*	45	

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V_{CC} V	Limit* 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 6)	f_{in} = 1MHz Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{OS}; Increase f_{in} Frequency Until dB Meter Reads –3dB; R_L = 50Ω, C_L = 10pF	3.0 4.5 5.5	 120 120 120	MHz
—	Off–Channel Feedthrough Isolation (Figure 7)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600Ω, C_L = 50pF	3.0 4.5 5.5	–50 –50 –50	dB
		f_{in} = 1.0MHz, R_L = 50Ω, C_L = 10pF	3.0 4.5 5.5	–37 –37 –37	
—	Feedthrough Noise. Channel–Select Input to Common I/O (Figure 8)	$V_{in} \leq$ 1MHz Square Wave ($t_r = t_f$ = 3ns); Adjust R_L at Setup so that I_S = 0A; Enable = GND R_L = 600Ω, C_L = 50pF	3.0 4.5 5.5	25 105 135	mV_{PP}
		R_L = 10kΩ, C_L = 10pF	3.0 4.5 5.5	35 145 190	
—	Crosstalk Between Any Two Switches (Figure 12)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600Ω, C_L = 50pF	3.0 4.5 5.5	–50 –50 –50	dB
		f_{in} = 1.0MHz, R_L = 50Ω, C_L = 10pF	3.0 4.5 5.5	–60 –60 –60	
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1kHz, R_L = 10kΩ, C_L = 50pF $THD = THD_{measured} - THD_{source}$ V_{IS} = 2.0V_{PP} sine wave V_{IS} = 4.0V_{PP} sine wave V_{IS} = 5.0V_{PP} sine wave	 3.0 4.5 5.5	 0.10 0.08 0.05	%

*Limits not tested. Determined by design and verified by qualification.

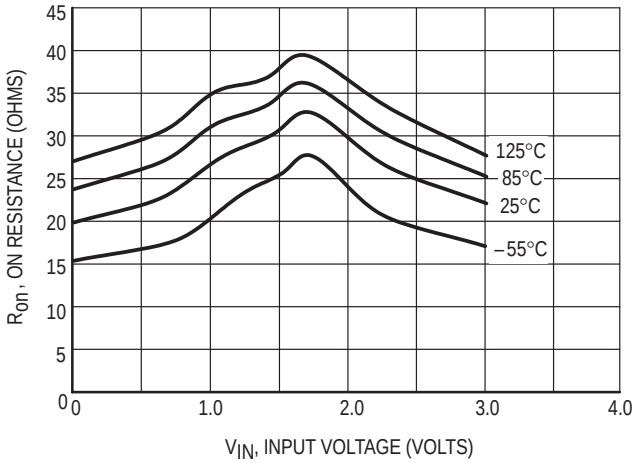


Figure 1a. Typical On Resistance, V_{CC} = 3.0 V

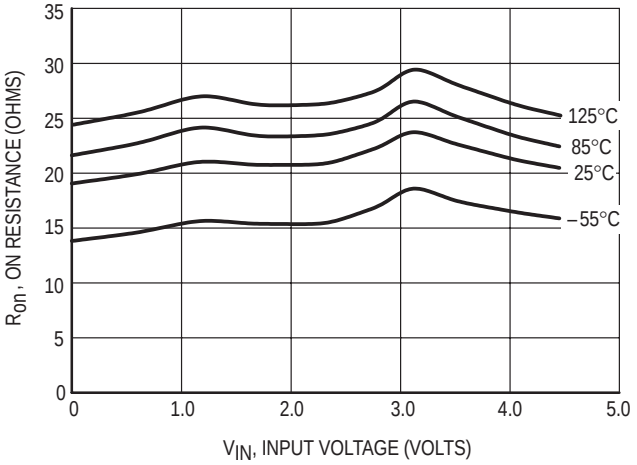


Figure 1b. Typical On Resistance, V_{CC} = 4.5 V

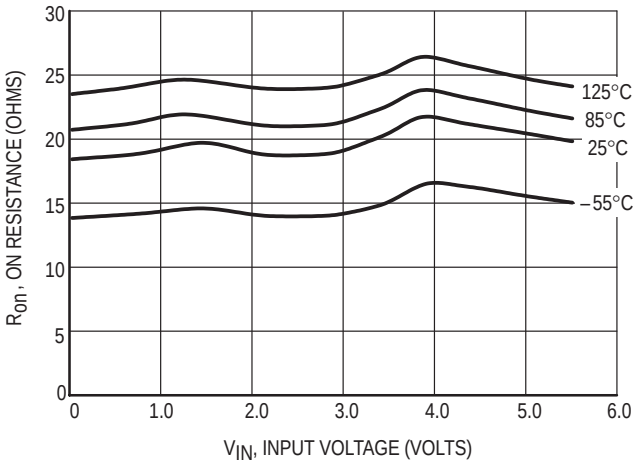


Figure 1c. Typical On Resistance, V_{CC} = 5.5 V

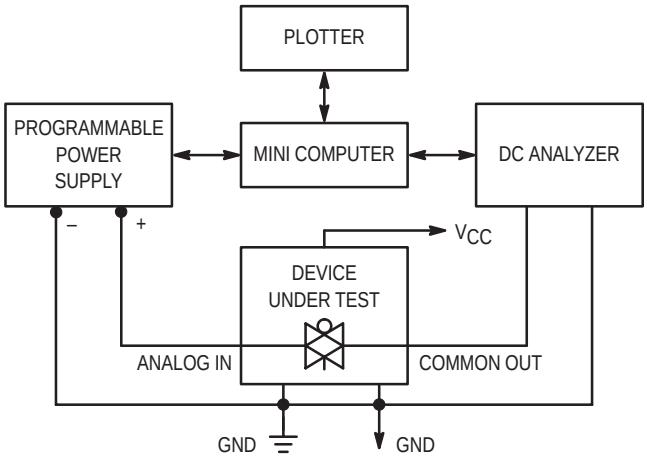


Figure 1. On Resistance Test Set–Up

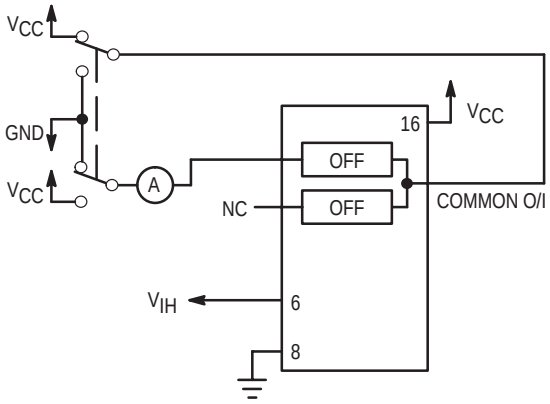


Figure 9. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

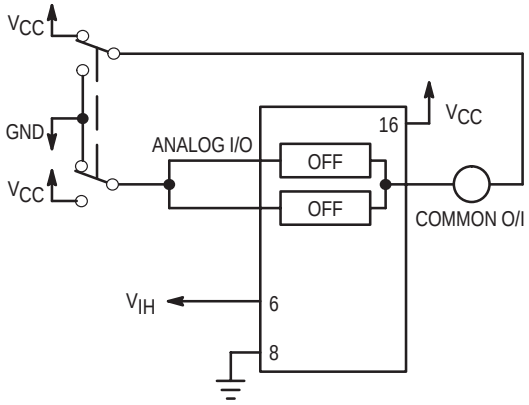


Figure 10. Maximum Off Channel Leakage Current, Common Channel, Test Set–Up

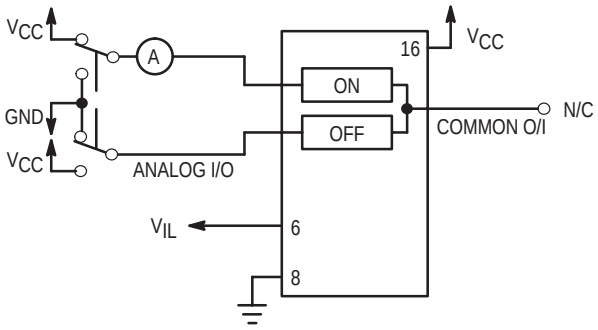
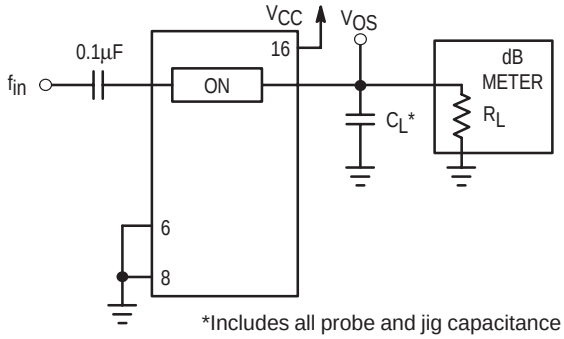
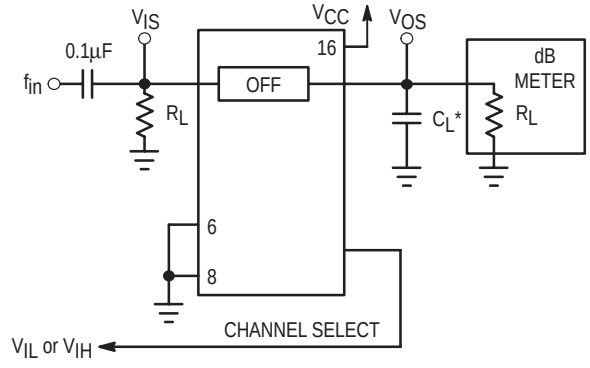


Figure 11. Maximum On Channel Leakage Current, Channel to Channel, Test Set–Up



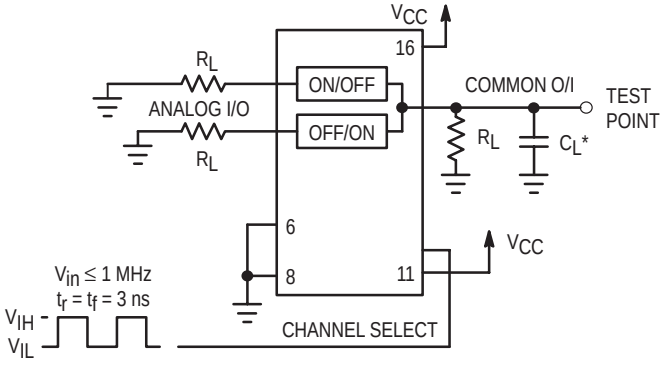
*Includes all probe and jig capacitance

Figure 12. Maximum On Channel Bandwidth, Test Set–Up



*Includes all probe and jig capacitance

Figure 13. Off Channel Feedthrough Isolation, Test Set–Up



*Includes all probe and jig capacitance

Figure 14. Feedthrough Noise, Channel Select to Common Out, Test Set–Up

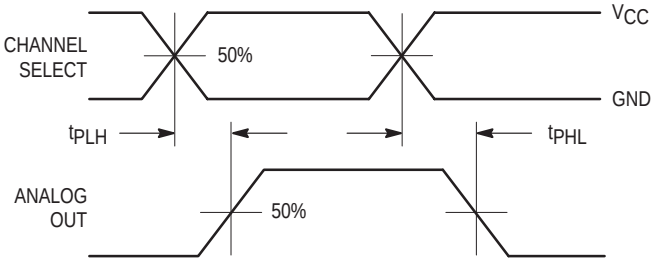
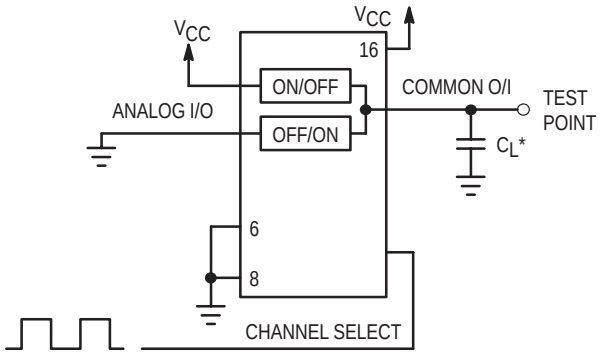


Figure 9a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 9b. Propagation Delay, Test Set–Up Channel Select to Analog Out

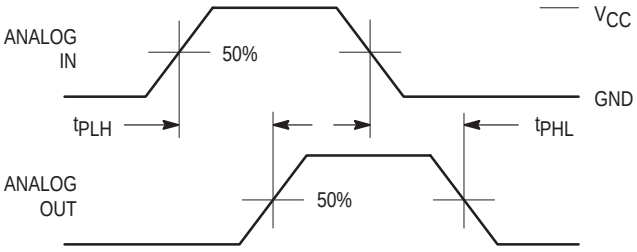
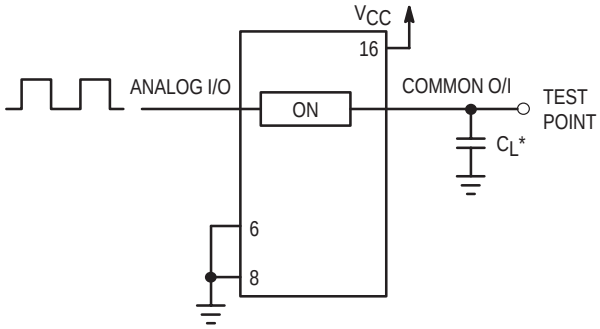


Figure 10a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 10b. Propagation Delay, Test Set–Up Analog In to Analog Out

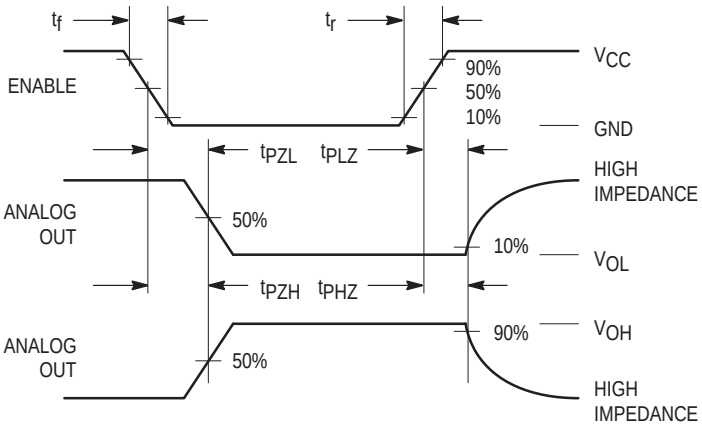


Figure 11a. Propagation Delays, Enable to Analog Out

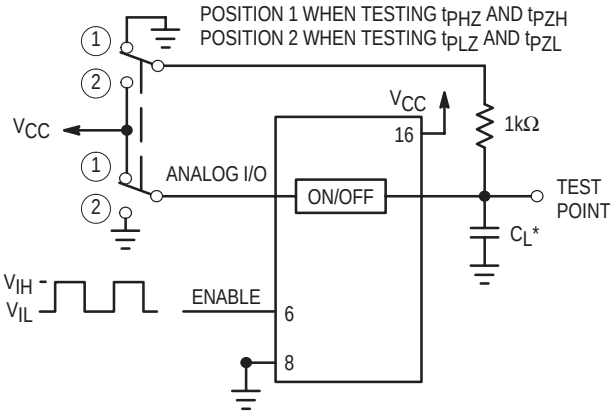


Figure 11b. Propagation Delay, Test Set–Up Enable to Analog Out

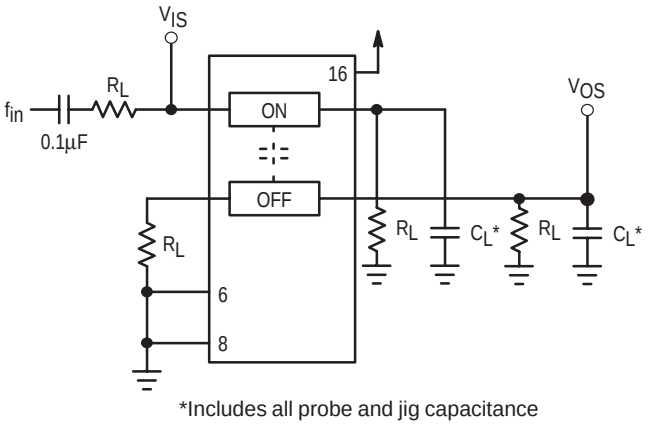


Figure 12. Crosstalk Between Any Two Switches, Test Set–Up

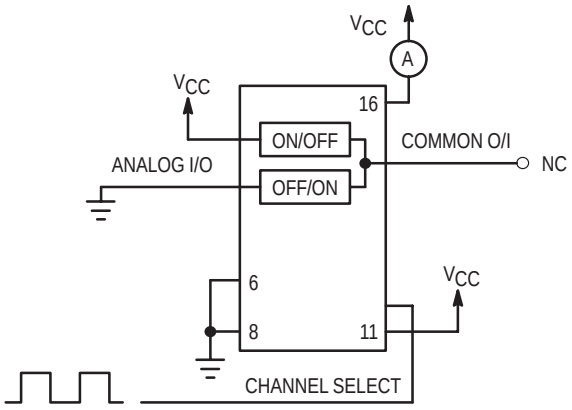


Figure 13. Power Dissipation Capacitance, Test Set–Up

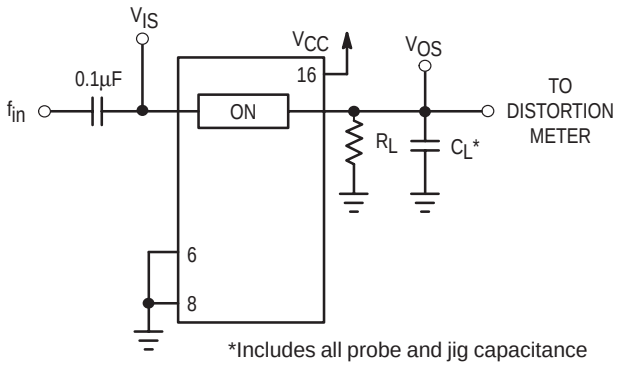


Figure 14a. Total Harmonic Distortion, Test Set–Up

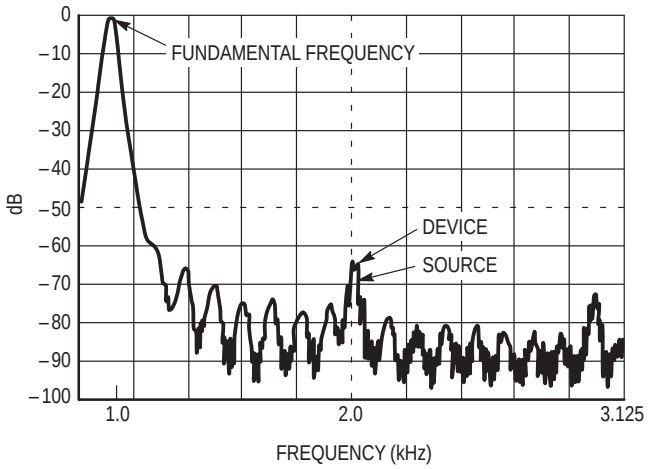


Figure 14b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

$$V_{CC} = +5V = \text{logic high}$$
$$GND = 0V = \text{logic low}$$

The maximum analog voltage swing is determined by the supply voltages V_{CC}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below GND. In this example, the difference between V_{CC} and GND is five volts. Therefore, using the configuration of Figure 15, a maximum analog signal of five volts peak–to–peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$V_{CC} - GND = 2 \text{ to } 6 \text{ volts}$$

When voltage transients above V_{CC} and/or below GND are anticipated on the analog channels, external Germanium or Schottky diodes (D_X) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

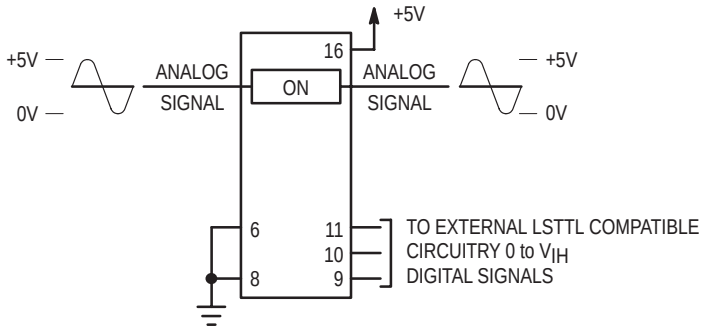


Figure 15. Application Example

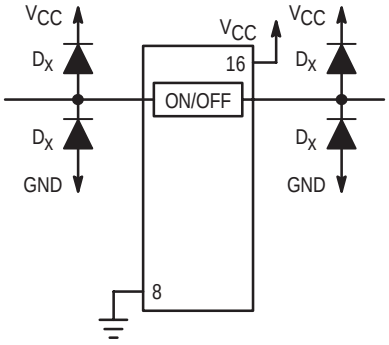
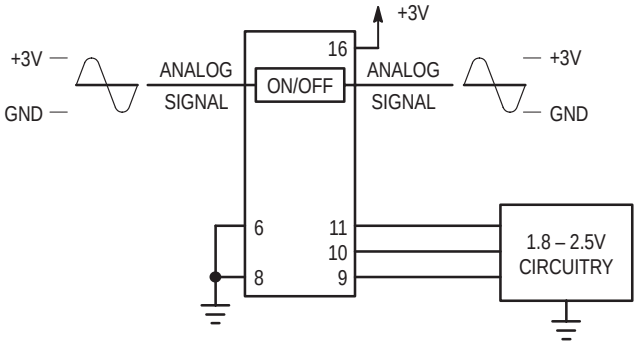
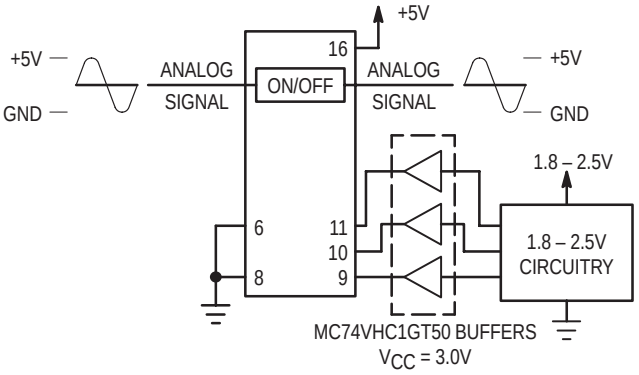


Figure 16. External Germanium or Schottky Clipping Diodes



a. Low Voltage Logic Level Shifting Control



b. 2–Stage Logic Level Shifting Control

Figure 17. Interfacing Low Voltage CMOS Inputs

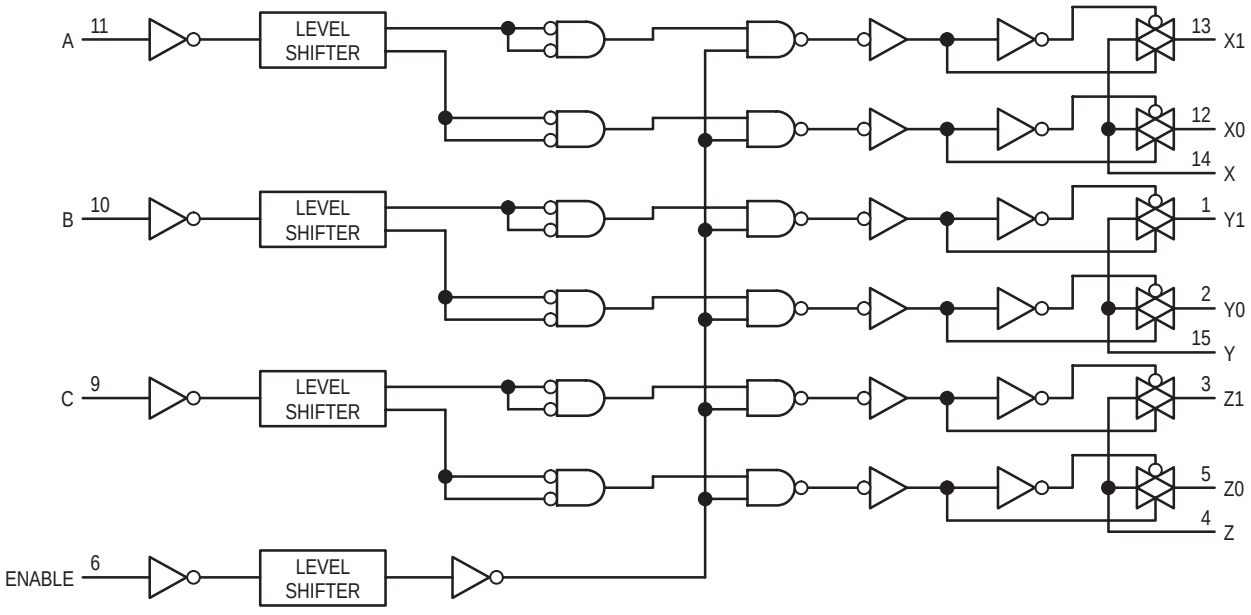
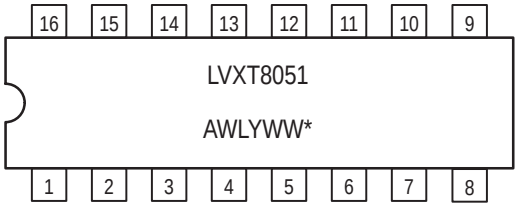
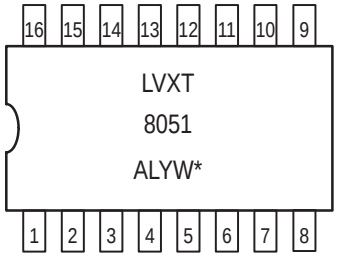


Figure 18. Function Diagram, LVXT8053

MARKING DIAGRAMS
(Top View)



16–LEAD SOIC
D SUFFIX
CASE 751B



16–LEAD TSSOP
DT SUFFIX
CASE 948F

*See Applications Note #AND8004/D for date code and traceability information.

Package Specifications and Case Outlines

TAPE & REEL SPECIFICATIONS

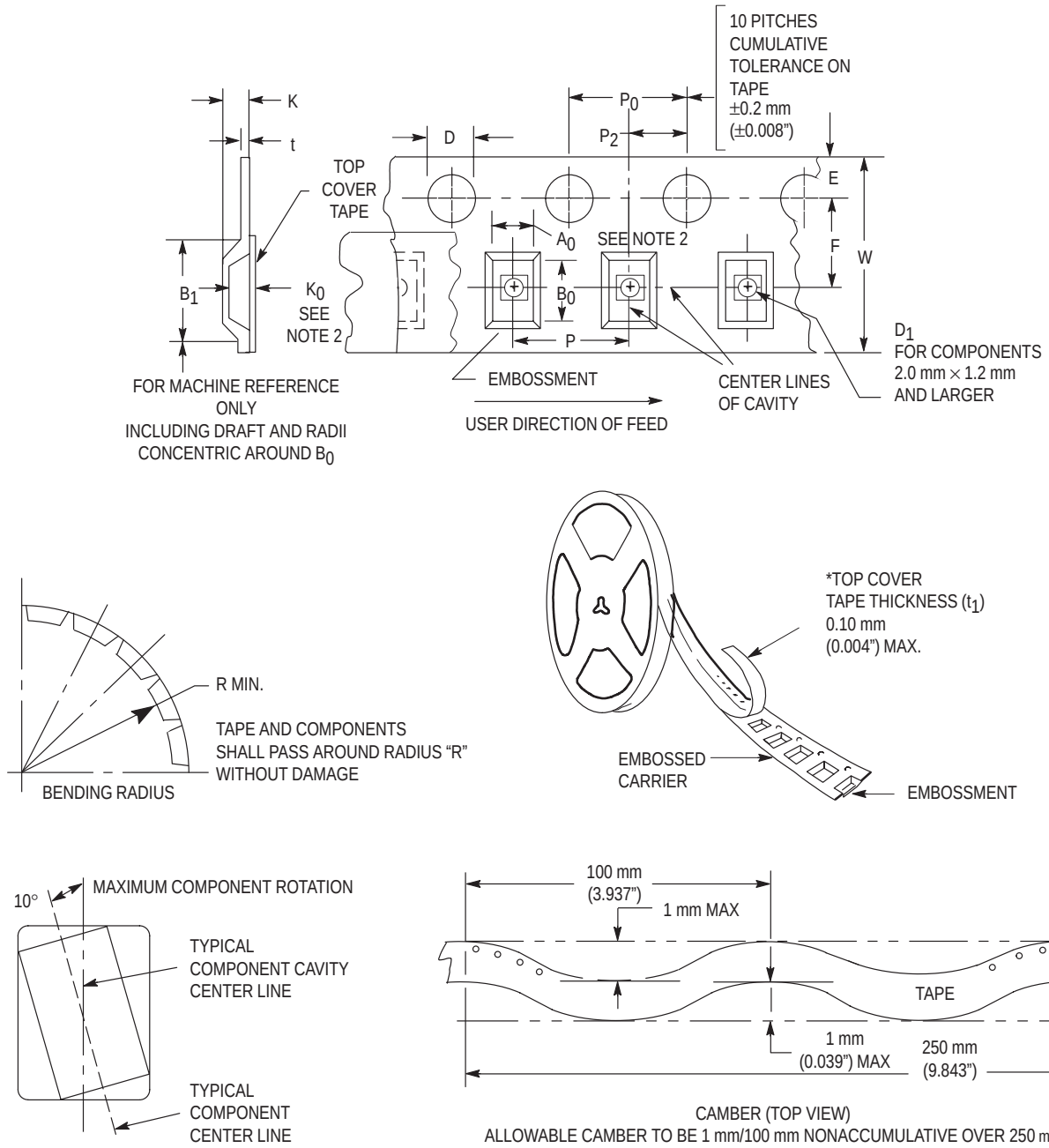


Figure 1. Carrier Tape Specifications

EMBOSSED CARRIER DIMENSIONS (See Notes 1 and 2)

Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R	T	W
8 mm	4.35 mm (0.171")	1.5 +0.1/ –0.0 mm (0.059 +0.004/ –0.0")	1.0 mm Min (0.039")	1.75 ±0.1 mm (0.069 ±0.004")	3.5 ±0.5 mm (1.38 ±0.002")	2.4 mm (0.094")	4.0 ±0.10 mm (0.157 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.1 mm (0.079 ±0.002")	25 mm (0.98")	0.3 ±0.05 mm (0.01 +0.0038/ –0.0002")	8.0 ±0.3 mm (0.315 ±0.012")

1. Metric Dimensions Govern–English are in parentheses for reference only.
2. A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

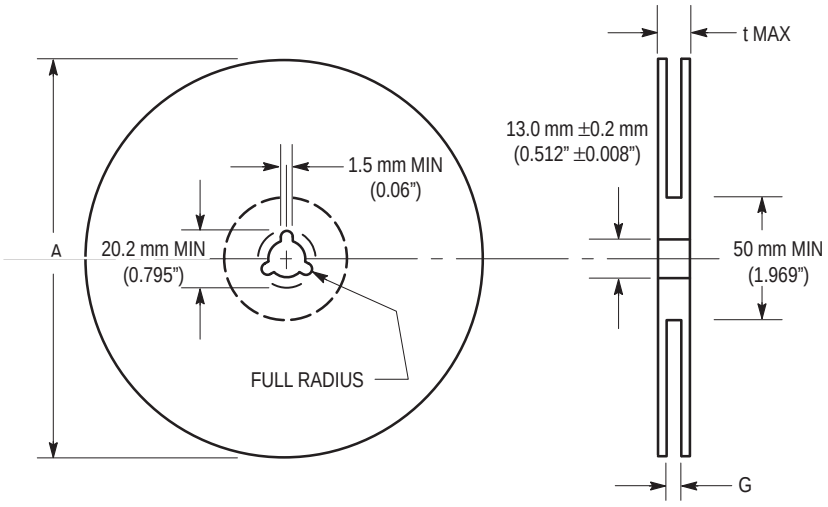


Figure 2. Reel Dimensions

REEL DIMENSIONS

Tape Size	A Max	G	t Max
8 mm	330 mm (13")	8.400 mm, +1.5 mm, –0.0 (0.33", +0.059", –0.00)	14.4 mm (0.56")

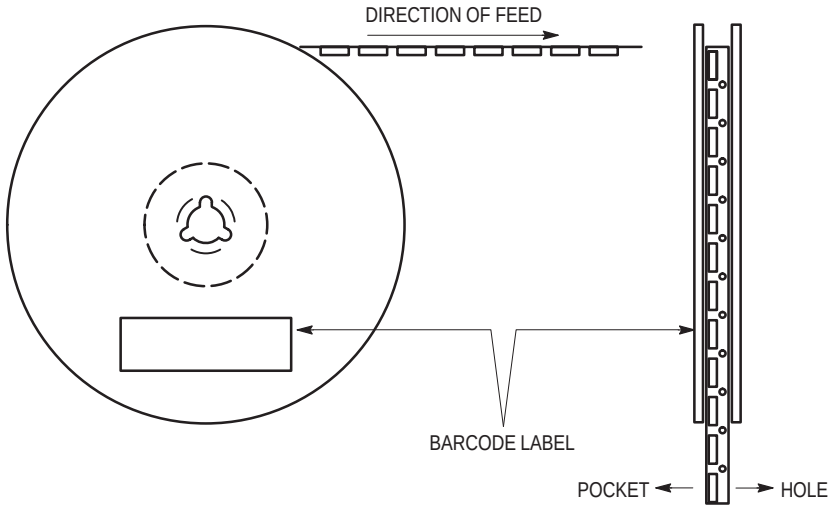


Figure 3. Reel Winding Direction

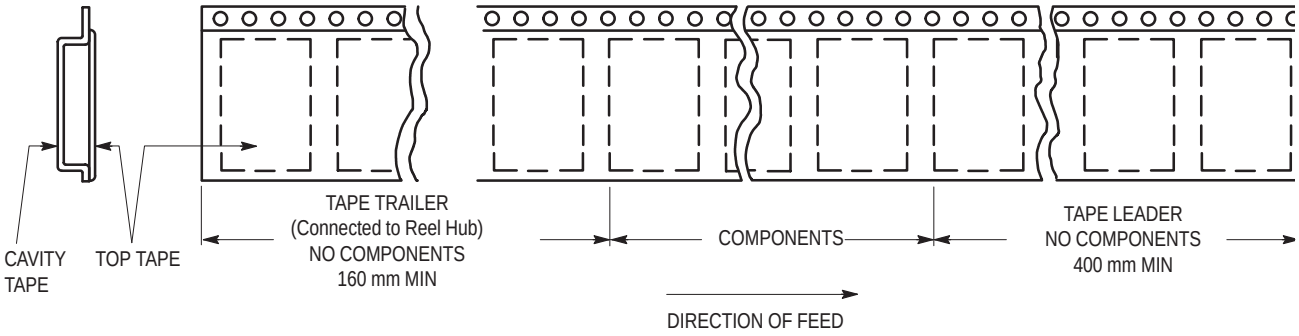


Figure 4. Tape Ends for Finished Goods

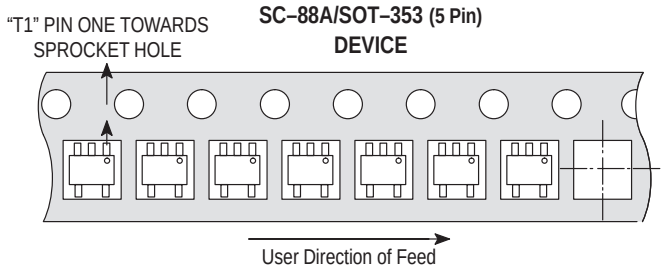
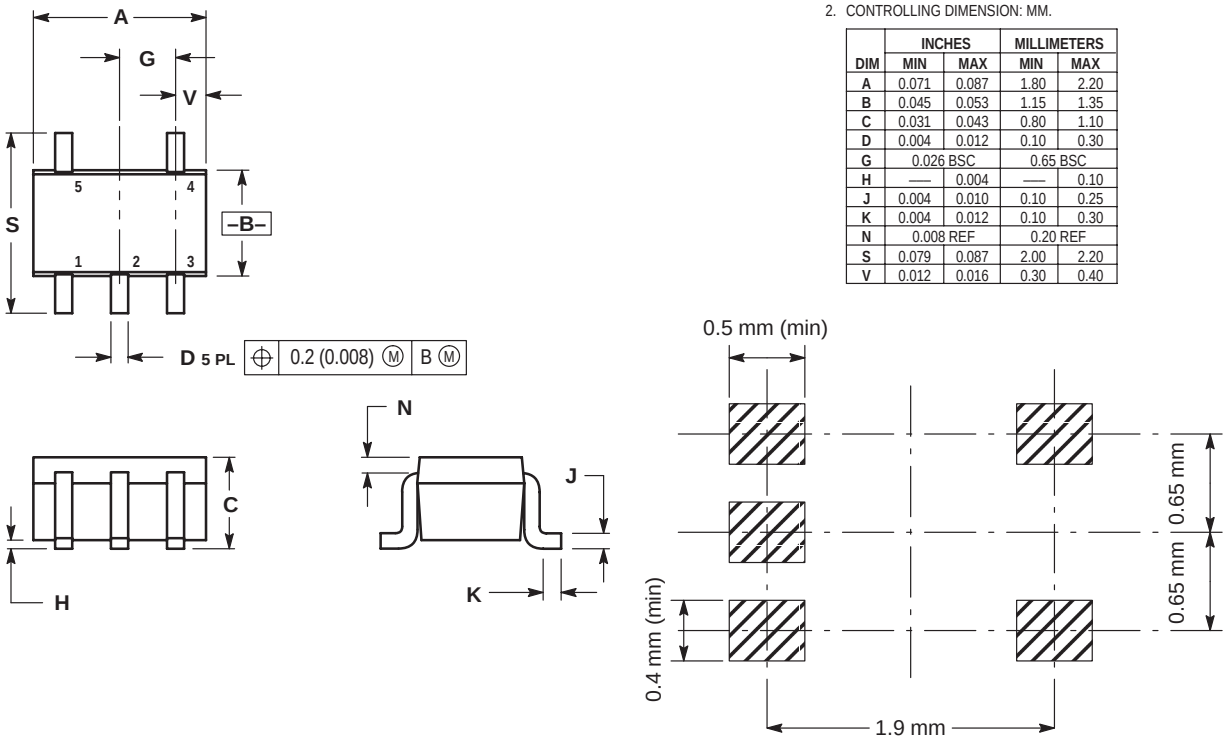


Figure 5. Reel Configuration

CASE OUTLINE AND PACKAGE DIMENSIONS

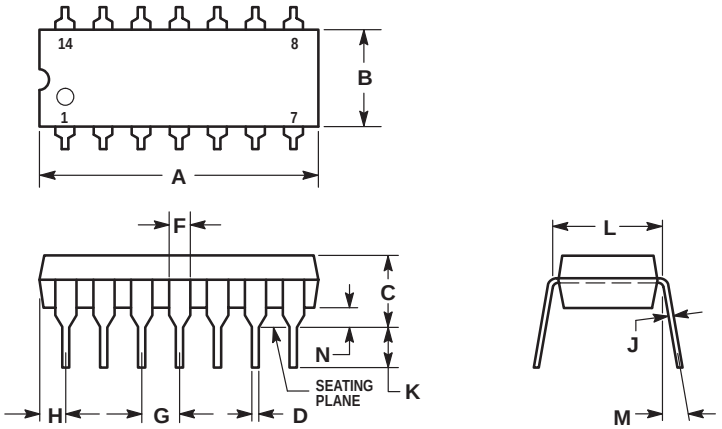
SC–88A / SOT–353
DF SUFFIX
5–LEAD PACKAGE
CASE 419A–01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	—	0.004	—	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

PDIP–14
P SUFFIX
PLASTIC DIP PACKAGE
CASE 646–06
ISSUE L

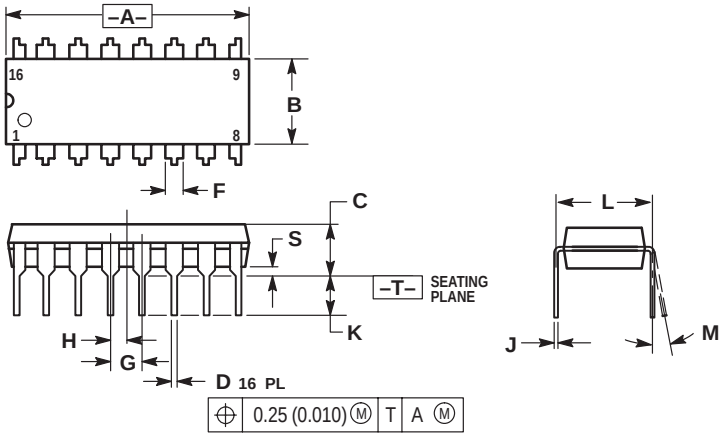


NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

CASE OUTLINE AND PACKAGE DIMENSIONS

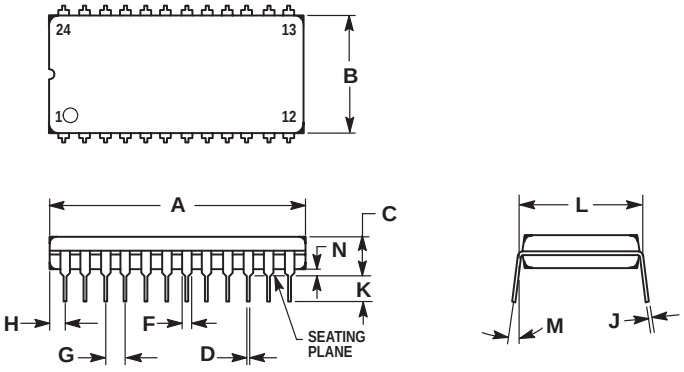
PDIP–16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

PDIP–24
P SUFFIX
PLASTIC DIP PACKAGE
CASE 709–02
ISSUE C

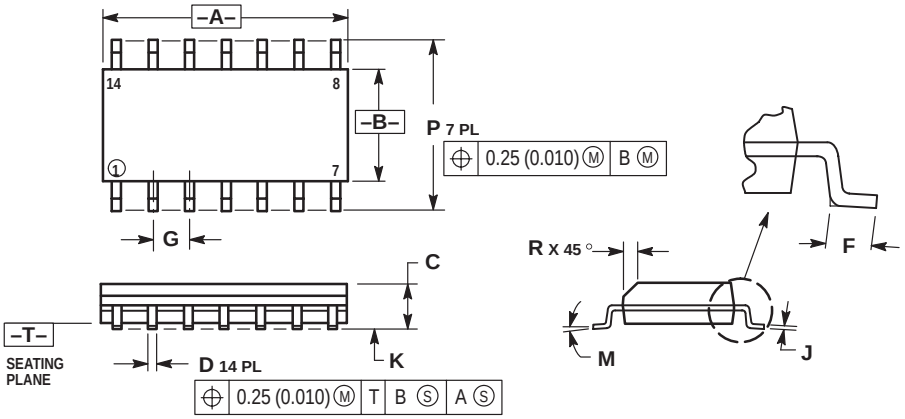


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0 °	15 °	0 °	15 °
N	0.51	1.02	0.020	0.040

CASE OUTLINE AND PACKAGE DIMENSIONS

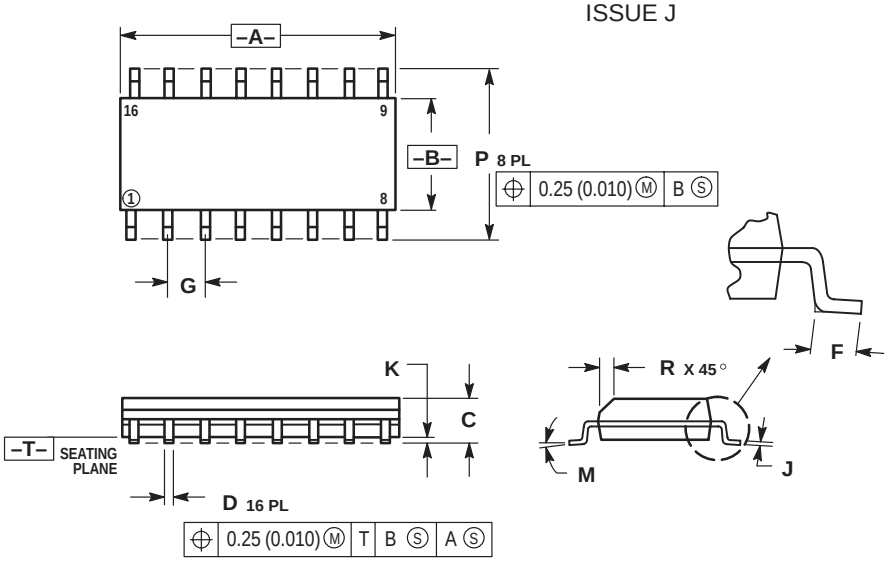
SO–14
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SO–16
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J

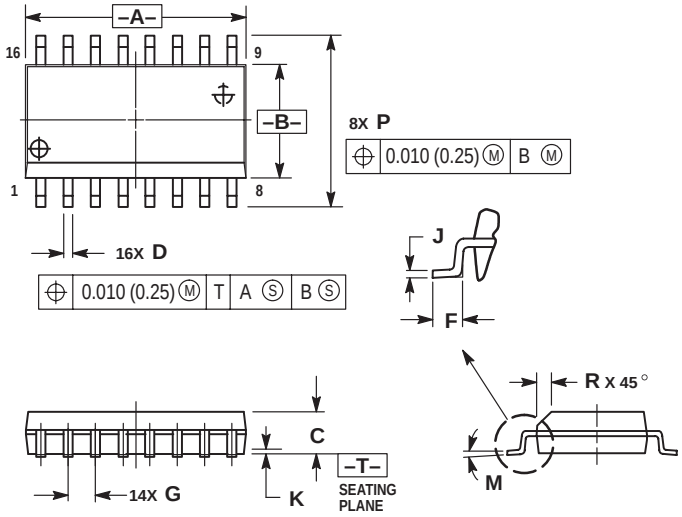


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

CASE OUTLINE AND PACKAGE DIMENSIONS

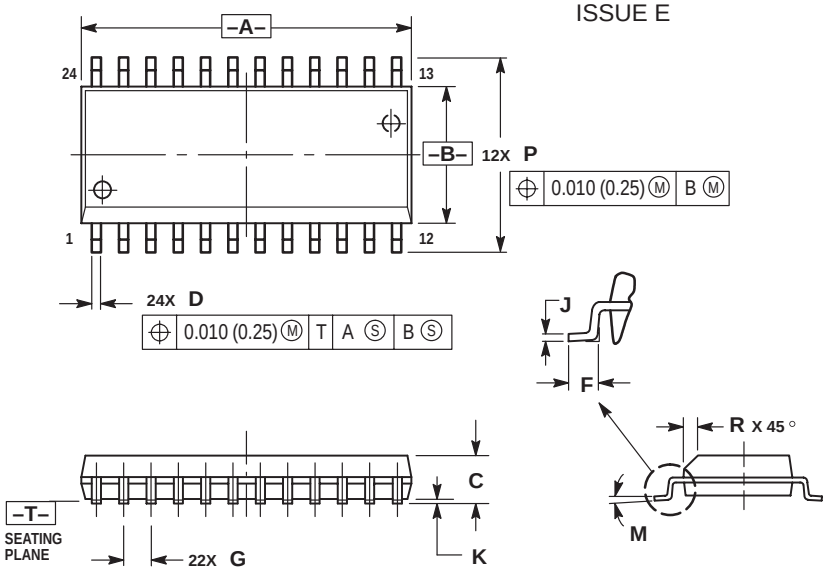
SO–16 WIDE
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751G–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

SO–24 WIDE
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751E–04
ISSUE E

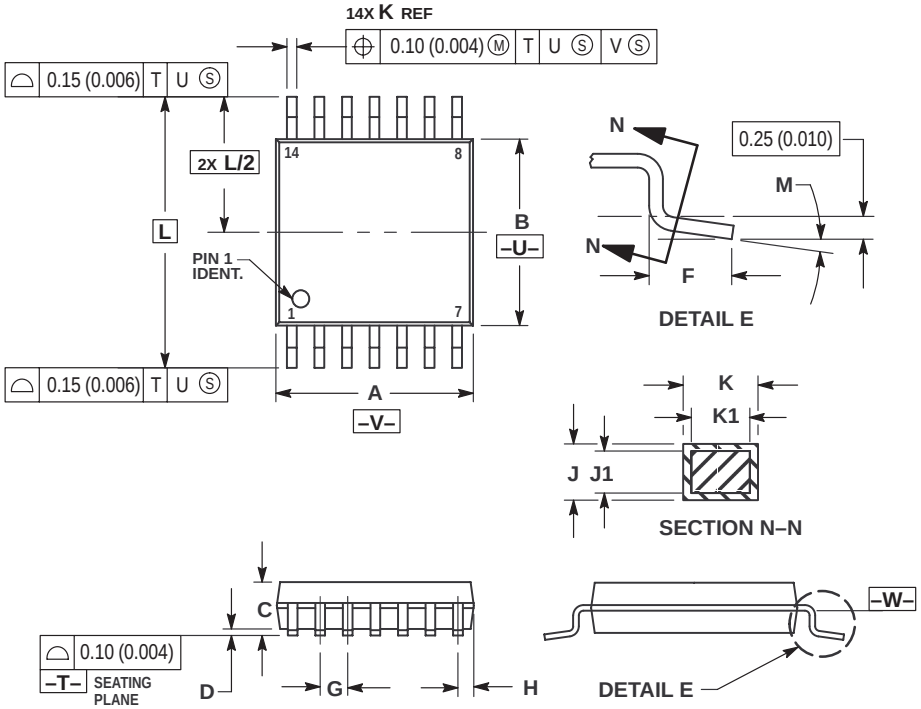


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0 °	8 °	0 °	8 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

CASE OUTLINE AND PACKAGE DIMENSIONS

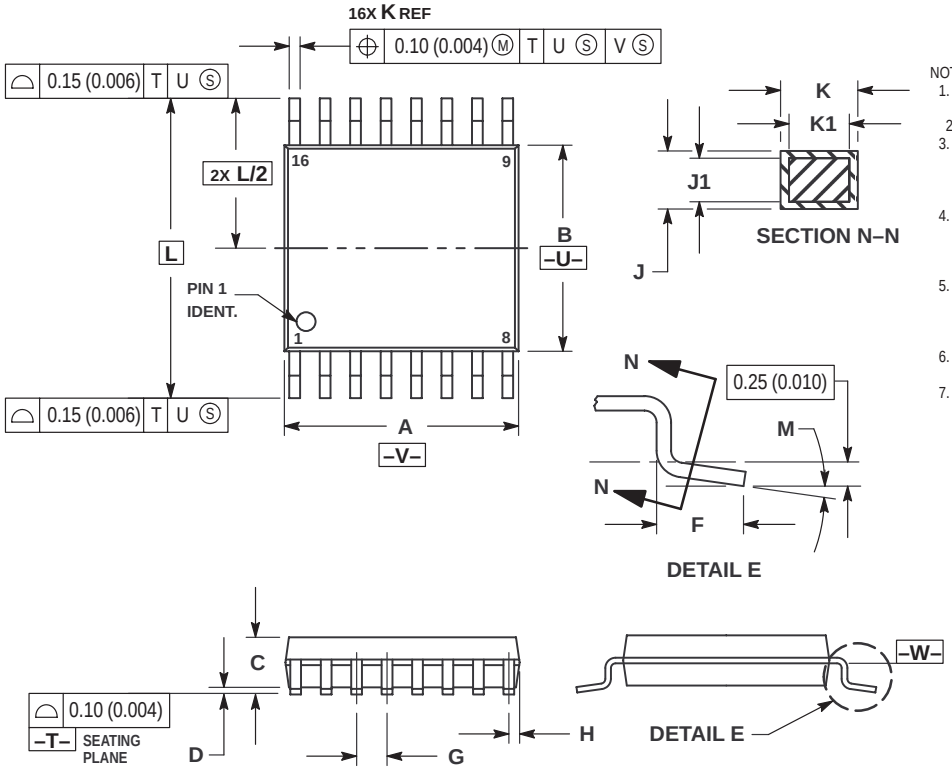
TSSOP–14
DT SUFFIX
CASE 948G–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

TSSOP–16
DT SUFFIX
CASE 948F–01
ISSUE O

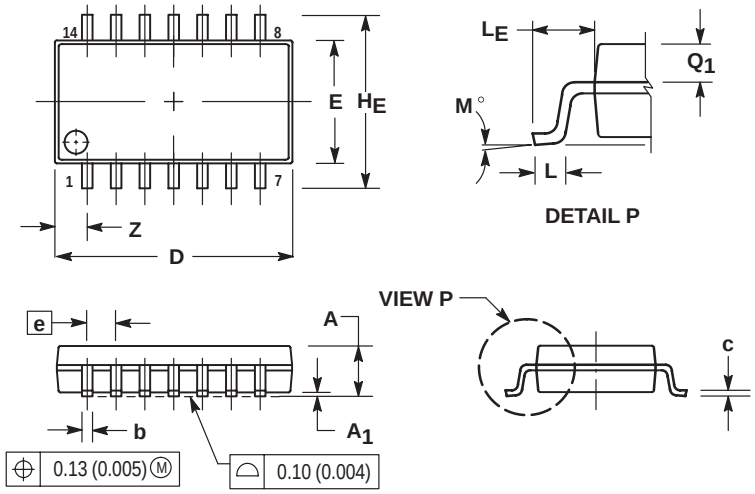


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

CASE OUTLINE AND PACKAGE DIMENSIONS

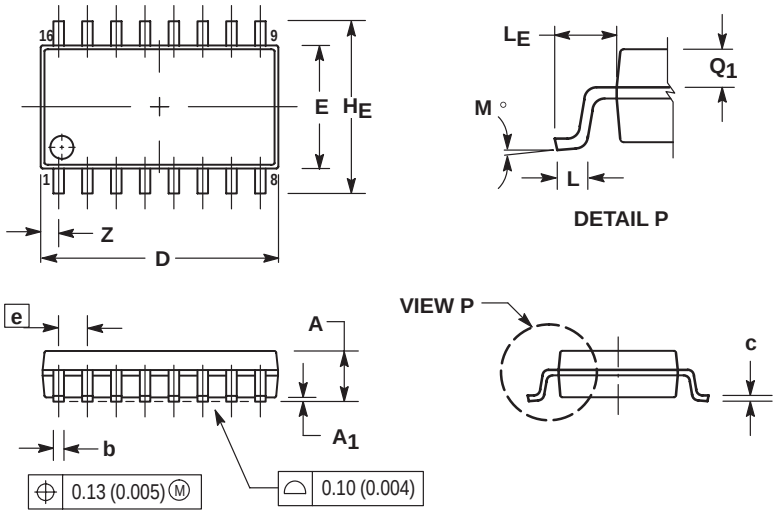
SO–14 EIAJ
F SUFFIX
CASE 965–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	—	1.42	—	0.056

SO–16 EIAJ
F SUFFIX
CASE 966–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
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	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	—	0.78	—	0.031

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* Majority of information (> 60%) is procedural, not functional, in nature
* Volume of information is typically less than for Reference Manuals
* Usually written more in active voice, using second–person singular (you) than is found in Reference Manuals
* May contain photographs and detailed line drawings rather than simple illustrations that are often found in Reference Manuals

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